NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA, G.B. NAGAR (AN AUTONOMOUS INSTITUTE)



Affiliated to

DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY, UTTAR PRADESH, LUCKNOW



Evaluation Scheme & Syllabus

For

Bachelor of Technology

Electronics Engineering (VLSI Design and Technology)

Second Year

(Effective from the Session: 2025-26)

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA, G.B. NAGAR (AN AUTONOMOUS INSTITUTE)

Bachelor of Technology Electronics Engineering (VLSI Design and Technology)

EVALUATION SCHEME SEMESTER-III

S.	Subject	Subject	Types of	Peri	iods		Evalu	ation	Schemes		Ei Sem	nd ester	Total	Credit
No.	Codes	Z dizgeet	Subjects	L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BCSCC0301	Employability Skill Development – I	Mandatory	2	0	0	60	40	100				100	2
2	BASL0301N	Technical Communication	Mandatory	2	0	0	30	20	50		50		100	2
3	BEC0301Z	Digital System Design	Mandatory	2	0	0	30	20	50		50		100	2
4	BEC0302Z	Analog Circuits	Mandatory	3	0	0	30	20	50		100		150	3
5	BEC0306	Data Structures	Mandatory	2	0	0	30	20	50		50		100	2
6	BECVL0301	VLSI Technology	Mandatory	3	0	0	30	20	50		100		150	3
7	BEC0351	Digital System Design Lab	Mandatory	0	0	4				50		50	100	2
8	BEC0352	Analog Circuits Lab	Mandatory	0	0	4				50		50	100	2
9	BEC0356	Data Structures Lab	Mandatory	0	0	2				25		25	50	1
10	BECVL0355	Linux and Scripting	Mandatory	0	0	6				50		100	150	3
11	BEC0359X	Social Internship	Mandatory	0	0	2				50			50	1
12	BNC0301/ BNC0302	Artificial Intelligence and Cyber Ethics / Environmental Science	Compulsory Audit	2	0	0	30	20	50					NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)												
		TOTAL		16	0	18			350	225	350	225	1150	23

* List of MOOCs Based Recommended Courses for Second year (Semester-III) B. Tech Students

Sr. No.	Subject Code	Course Name	University / Industry Partner Name	No of Hours	Credits
1	BMC0012	Data Structures and Algorithms using Python - Part 1	Infosys Wingspan (Infosys Springboard)	29h 27m	2
2	BMC0020	Express PCB Training	Infosys Wingspan (Infosys Springboard)	15h 6m	1

PLEASE NOTE: -

- A 3-4 weeks Internship shall be conducted during summer break after semester-II and will be assessed during semester-III
- Compulsory Audit (CA) Courses (Non-Credit BNC0301/BNC0302)
 - All Compulsory Audit Courses (a qualifying exam) do not require any credit.
 - > The total and obtained marks are not added in the grand total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses.

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA, G.B. NAGAR (AN AUTONOMOUS INSTITUTE)

Bachelor of Technology Electronics Engineering (VLSI Design and Technology)

EVALUATION SCHEME

SEMESTER-IV

Sl.	Subject	Subject	Types of	P	Perio	ls		Evalua	tion Scheme	es		nd ester	Total	Credit
No.	Codes		Subjects	L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BASCC0401	Employability Skill Development - II	Mandatory	2	0	0	60	40	100				100	2
2	BECVL0401	Analog and Digital Signal Processing & Communication	Mandatory	3	0	0	30	20	50		100		150	3
3	BECVL0402	CMOS Analog Integrated Circuit	Mandatory	3	0	0	30	20	50		100		150	3
4	BEC0402N	Microprocessor & Microcontroller	Mandatory	3	0	0	30	20	50		100		150	3
5		Departmental Elective 1	Departmental Elective	3	0	0	30	20	50		100		150	3
6	BAS0403	Advance Engineering Mathematics	Mandatory	3	1	0	30	20	50		100		150	4
7	BEC0452	Microprocessor & Microcontroller Lab	Mandatory	0	0	4				50		50	100	2
8	BECVL0452	CMOS Analog Integrated Circuit Lab	Mandatory	0	0	2				25		25	50	1
9	BEC0455	Verilog-HDL	Mandatory	0	0	6				50		100	150	3
	BCSCC0452	Problèm Solving Approches	Mandatory	0	0	2				50			50	1
10	BEC0459	Mini Project	Mandatory	0	0	2				50			50	1
12	BNC0402/ BNC0401	Environmental Science / Artificial Intelligence and Cyber Ethics	Compulsory Audit	2	0	0	30	20	50				50	NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)												
		TOTAL		19	1	16			350	225	500	175	1250	26

* List of MOOCs Based Recommended Courses for Second year (Semester-IV) B. Tech Students

S. No.	Subject Code	Course Name	University / Industry Partner Name	No of Hours	Credits
1	BMC0080	Hardware Description Languages for FPGA Design	Infosys Wingspan (Infosys Springboard)	36h 15m	3
2	BMC0023	Internet of Things 201	Infosys Wingspan (Infosys Springboard)	15h 59m	1
3	BMC0021	IoT Raspberry Pi with Projects	Infosys Wingspan (Infosys Springboard)	12h 25m	0.5

PLEASE NOTE: -

- A 3-4 weeks Internship shall be conducted during summer break after semester-IV and will be assessed during Semester-V
- Compulsory Audit (CA) Courses (Non-Credit BNC0401/BNC0402)
 - ➤ All Compulsory Audit Courses (a qualifying exam) do not require any credit.
 - The Total and obtained marks are not added in the Grand Total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses.

List of Departmental Electives

Sr. No.	Departmental Electives	Subject Codes	Subject Name	Bucket Name
1	Elective-I	BECVL0412	Data Analytics	AI & ML
2	Elective-I	BECVL0413	IoT Architecture and Protocols	Embedded & IoT
3	Elective-I	BECVL0411	Compound Semiconductor	Semiconductor Devices & Display Technologies

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA, GAUTAM BUDDH NAGAR (AN AUTONOMOUS INSTITUTE)

AICTE Guidelines in Model Curriculum:

A student will be eligible to get Under Graduate degree with Honours only, if he/she completes the additional MOOCs courses such as Coursera certifications, or any other online courses recommended by the Institute (Equivalent to 20 credits). During Complete B.Tech. Program Guidelines for credit calculations are as follows.

1.	For 6 to 12 Hours	=0.5 Credit
2.	For 13 to 18	=1 Credit
3.	For 19 to 24	=1.5 Credit
4.	For 25 to 30	=2 Credit
5.	For 31 to 35	=2.5 Credit
6.	For 36 to 41	=3 Credit
7.	For 42 to 47	=3.5 Credit
8.	For 48 and above	=4 Credit

For registration to MOOCs Courses, the students shall follow Coursera registration details as per the assigned login and password by the Institute these courses may be cleared during the B. Tech degree program (as per the list provided). After successful completion of these MOOCs courses, the students shall provide their successful completion status/certificates to the Controller of Examination (COE) of the Institute through their coordinators/Mentors only.

The students shall be awarded Honours Degree as per following criterion.

- i. If he / she secures 7.50 as above CGPA.
- ii. Passed each subject of that degree program in the single attempt without any grace.
- iii. Successful completion of MOOCs based 20 credits.

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Course (Offered i	n: B.Tech	1										2	0	0	2
Pre-requ	iisite: Pr	grammin	g Langua;	ge C												
Course	Objectiv	es: This	course in	ntroduce	s compu	ter syste	em fund	amental	s, basic	mathema	atics for	comp	outing	, and	l soft	twa
								while	creating	real-wo	rld appl	icatio	ns, m	ini-g	ames,	, ar
Course (Outcome	: After co	mpletion of	of the co	urse, the	student	will be a	ble to								ledg
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CO1														K	.3	
CO2			nplement	the step	s in the s	oftware	developi	nent life	cycle us	sing logic	al reasor	ning		K	3	
002					_											
CO3	_		•	-scale so	oftware p	projects	or game	s using	structure	ed progra	amming	and		K	6	
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CO4						ı presen	t a com	piete soi	itware p	roject, ac	emonstra	ung		K	6	
Pre-requisite: Programming Language C Course Objectives: This course introduces computer system fundamentals, basic mathematics for computing, and software development principles. It emphasizes algorithm design and C++ programming skills. Through hands-on practice and project-based learning, students develop problem-solving abilities and teamwork while creating real-world applications, mini-games, and simulations, enhancing both technical and collaborative competencies Course Outcome: After completion of the course, the student will be able to CO1 Apply sets, relations, functions to computational problem-solving CO2 Understand and implement the steps in the software development life cycle using logical reasoning and flowcharts. CO3 Design and develop small-scale software projects or games using structured programming and project-based approaches. CO4 CO4 CO5 Design and develop small-scale software projects or games using structured programming and project-based approaches. CO6 CO6 CO6 CO7																
Course Offered in: B.Tech Pre-requisite: Programming Language C Pre-requisite: Programming Language C Course Objectives: This course: introduces computer system fundamentals, basic mathematics for computing, and software development principles. It emphasizes algorithm design and C++ programming skills. Through hands-on practice and project-based learning, students develop problem-softing and teamwork while creating real-world applications, mimi-games simulations, enhancing both technical and collaborative competencies Course Outcome: After completion of the course, the student will be able to Blowm's Knew Course (RL)																
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CO2	3	3	3	2	-	-	-	2	-	_	_	-		-		-
CO3	2	3	3	2				2								
			_	1			-		_		_					
CO4	3	3	3	3	-	-	-	2	-	-	-	-		-		-
Course (Contents	/ Syllabu	S													
Module	1		Fou	ındation	s of Con	nputer S	ystems	and Ma	thematic	cal Conc	epts			4	l hou	rs
Comput	er Systei	ı Fundan	nentals: In	ntroducti	on to Ass	sembler,	Compile	r. Interp	reter, Ro	le of Load	der and L	inker i	in pro	gram	execu	ıtioı
Mathem	atical Fo	undation	s for Con	nputing:	Sets, Re	elations,	-	-	efinition	s and app	lications	, Princ	ciple o	of Ma	them	atica
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Course Name: Employability Skill Development – I

Course Code: BCSCC0301

Course Code	: BASL03	301N			Course I	Name: 7	Technic	al Com	municat	tion			L T	P C
Course Offer	red in: B.	Tech. A	ll branc	ches (ex	cept CS	BS)							2 0	0 2
Pre-requisite	: Interme	diate le	vel (CE	FR) and	d above	•						<u>, </u>		
Course Obje	ctives:													
	onstrate							ion skill	s in dive	erse profe	essional s	ettings, i	ncluding	
	tings, pres			-										
	elop and a							te writt	en comi	municati	on, such	as email	s, letters,	
	nos, resum pt comm ı							nal and	l cituati	onal con	toyte to f	oster inc	luciva	
	respectful					ai, oi ga	mzano	mai, am	ı sıtuatı	onai con	icais to 1	oster inc	iusive	
	oloy digita					atforms	(e.g., v	ideo cor	nferenci	ng, busin	ess messa	aging ap	ps) respo	nsibly
	effectively													
Course Outc	ome: Afte	er comple	etion of	the cou	rse, the s	student v	vill be a	ble to						
	end the pr													
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CO-PO Map							ir digital	modiu.						
СО-РО		T		,										
Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	1	1	1	1	1	2	1	1	2	3	1	2	-	-
CO2	1	1	1	1	1	1	1	1	2	3	1	2	-	-
CO3	1	1	1	1	1	1	1	1	2	3	1	2	-	-
CO4	1	1	1	1	1	1	1	1	2	3	1	2	-	-
CO5	1	1	1	1	1	1	1	1	2	3	1	2	-	-
Course Cont	ents / Syll	abus		1	1		1	I	1	1	1	1	1	I
Module 1			Intro	duction	to Tecl	nical C	ommui	nication	ļ				4 Hours	
											. ~		_	
Technical Co													tion: emp	ohasis on
gender neutra	l language	and cul				icance (of audie	ence in t	echnica	ıl commu	inication	,	<i>-</i>	
Module 2			1 ecn	nical W	riting 1								5 Hours	
Technical wr	iting skill	: charac	teristics	, examp	les; Bus	iness le	tters/en	nails: C	ontent o	rganizatio	on, Tone	and inte	nt; Agen	da &
Minutes of M	_													
Module 3			Tech	nical W	riting 2								5 Hours	
Job applicati	on Dogu	ma': Da	out nu	opogoli	Toohni	ool non	om: A bat	root. Et	higal W	nitings C	ony Edit	ing Dof	ranaina	and
Plagiarism	ion, Kesui	ше , кер	ort, pr	oposai,	1 eciliii	cai pape	er. Aust	raci, Ei	ilicai vv	riung. C	opy Eun	ilig, Keit	ereneing	anu
Module 4		-	Publi	ic Speak	ring .								6 Hours	
Components	of effecti	ve sneak				halance	in arran	oing ide	as Imn	ortance o	f KOPP			for a iol
interview: FA		_	_			outunee	iii airai	igilig ide	cas. Imp	ortunee o	IKOIII	101, 1 ip	pearing	101 a joi
	100, 1010	phome (ote Con	nmunica	ation						4 Hours	
vioquie 5	1:	latforms						te: emai	lide ne	ernames:	Writing			g Vlogs
Module 5 Remote worl	(՝ Որրոբ ո	Tati OIIIIS	, viuco	Comer	menig,	· II tual	cuquet	cc. ciiiai	1103, 03		Lecture 1		24 Hour	
Module 5 Remote worl	k: online p									I Juli I		LUUIS	IIUuI	
Remote worl	k: online p													
Remote work Textbook:		itle with	n public	cation a	gencv &	vear				Autho	r			
Remote work Textbook: S.No	Book T	Title with	_		•	-	4 th Edit	ion by N	Meenaks	Autho		eeta Sha	rma, Oxf	ord Univ
Textbook: S.No 1. Tecl		nmunica	tion – F		•	-	4 th Edit	ion by N	Meenaks			eeta Sha	rma, Oxf	ford Univ
Textbook: S.No 1. Tecl	Book T nnical Cor s, 2022, N	nmunica	tion – F		•	-	4 th Edit	ion by N	Meenaks			eeta Sha	rma, Oxf	ord Univ

- 1. Technical Communication, 15th Edition by John M. Lannon & Laura J. Gurak, Pearson, 2021.
- 2. Spoken English- A Manual of Speech and Phonetics (5th Edition) by R K Bansal & J B Harrison, Orient Blackswan, 2024, New Delhi.
- 2024, New Delhi.

 th

 Business Correspondence and Report Writing by Prof. R C Sharma, Krishna Mohan, and Virendra Singh Nirban (6 Edition), Tata McGraw Hill & Co. Ltd., 2020, New Delhi.

Intercultural Communication in Virtual Exchange by Francesca Helm, Cambridge Univ. Press, 2024.

NPTEL/ You	u tube/ Faculty Video Link:
Module 1	https://onlinecourses.nptel.ac.in/noc24_ge37/preview
Module 2	https://archive.nptel.ac.in/courses/109/106/109106094/
Module 3	https://www.youtube.com/watch?v=kOJlwMJxEG0&t=8s
Module 4	https://www.youtube.com/watch?v=Sg7Q_dC_fWU&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb
Module 5	https://www.youtube.com/watch?v=ymLFJDpjgCk&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb&index=6

					Cor	urse Na	me: D	igital Sy	ystem l	Design				L '	ГР	C
Course	Offered i	n: EE/V	/LSI											2	0 0	2
Pre-req	uisite: Ba	sics con	cept of a	arithmeti	c opera	tions, B	asic of	decimal	numbe	er syste	m					
Course	Objective	es:The st	tudent w	ill learn	about B	oolean	algebra	, logic f	unction	minim	nization	by K ma	ıp, binar	y codes, I	Designin	g an
analysis	of combi	national	and seq	quential	circuits,	Synch	ronous	& Asyn	chrono	us Seq	uential (Circuits,	Semico	nductor 1	nemorie	s ar
program	mable log	gic devic	es.													
Course	Outcome	: After o	completi	on of the	course	, the stu	ident wi	ll be ab	le to					Bloom	's Know	led
														Level (KL)	
CO1	Verify t	he logic	operation	ons and a	pply th	e optim	ization	techniqu	ues to i	mplem	ent logic	functio	ns.		K3	
CO2	Design	and anal	lyze com	bination	al logic	circuit	s.								K4	
CO3	Explain	differer	nt types o	of flip-fl	ops and	apply t	o imple	ment se	quentia	ıl circui	its.				К3	
CO4	Design	and anal	lyze Syn	chronou	s & Asy	nchron	ous Seq	uential	Circuit	s.					К3	
~~=	Explain	the con	cept of S	Semicon	ductor N	/Jemori	es and i	mpleme	nt the c	ligital l	ogic fun	ctions u	sing			
CO5	PLDs.		-					-							K3	
CO-PO	Mapping	(Scale	1: Low,	2: Med	ium, 3:	High)								1		
CO DO	<u>, </u>	<u> </u>														
		O 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3	ţ
	···s															
CO1		3	3	2	-	-	-	-	-	-	-	2	3	2	2	
Course Offered in: EE/VLS Series concept of arithmetic operations, Basic of decimal number system 2 0 0																
CO3		3	3	2	-	-	-	-	-	-	-	2	3	2	2	
				2	_	_	_	_	_	_	_	2		2	2	
			_	2	-	-	-	-	-	-	-	2	3	2	2	
		/ Syllab														
															II.	
												c Gates,	SOP &	POS Fori	ns, Cano	onic
		Maps uj							ations,	Binary	Codes.				10 ha	
										1 41	1 4 1			TT 10 0		
														Half Su	btractor.	, Fu
		And Pa								ters, Er	icoders,	and De	coders.		10 ha	
		. F da								1:1 CD) T -4-1-	Dia Dia	CD 1	W IV M		
		-				nes rue	or un	i i iip i i	ops, c	JII V C151	on nom	one typ	or ring	1 lop to	unother.	511
						Asyno	hronou	ıs Sequ	ential (Circuit	s				12 ho	urs
Synchro	nous Seq	uential (Circuits:	Design	and an	alysis	of clock	ed sequ	uential	circuit	s, state	reductio	n and a	ssignmen	ts, Desi	gn
sequenc	e detector	and Co	unter.					-								_
Asynch	onous Sec	quential	Circuits	: Design	and ana	alysis o	f asynch	ronous	sequen	tial circ	cuits, cir	cuit with	h latches	, reductio	n of sta	ie a
flow tab	le, race-fr	ee state	assignm	ent, haza	ards.											
Module	5			Progran	nmable	Logic	Devices	i							8 hou	rs
Semico	nductor M									M, comp	arison, I	Designin	g a			
circuit i	mplement	ation usi	ing prog	rammab	le logic	devices	: PRON	I, PAL,	PLA,	Introdu	ction of	CPLD a	and FPG	A.		-
												Tota	l Lectui	e Hours	48 ho	urs
Textboo)k:														_1	
S.No		Title wi	ith publi	ication a	gency	& year					Aut	hor				
1	"Mod	ern digit	tal Electr	ronics",	Tata Mo	Graw I	Hill, 4th	edition	, 2009.		R.P	. Jain				
											M. 1	Morris I	Mano an	d Michae	l D. Cile	tti
	_		- '								I					
2	ce Books	•														
2	ce Books	•														

1	Digital Design: Principles and Practices, Pearson, (2000).	John F Wakerly
2	"Digital Electronics- An introduction to theory and practice", PHI, 2ndedition ,2006.	W.H. Gothmann
3	"Theory and Logic Design", PHI, 2013.	A. Anand Kumar
NPTEL/	Youtube/ Faculty Video Link:	
Unit I	https://www.youtube.com/watch?v=juJR JDJRa0	
	https://www.youtube.com/watch?v=2cpl HjcI3A	
	https://www.youtube.com/watch?v=KergVtV3SxU	
	https://www.youtube.com/watch?v=kgL5UaSVuro	
	https://www.youtube.com/watch?v=EznCqZ1eh5Q	
Unit II	https://www.youtube.com/watch?v=sUutDs7FFeA	
	https://www.youtube.com/watch?v=XCiLHOZsQl8	
Unit III	https://www.youtube.com/watch?v=ibQBb5yEDlQ	
	https://www.youtube.com/watch?v=LHAbLXfRYXk	
	https://www.youtube.com/watch?v=Gc3DL-tmr-g	
	https://www.youtube.com/watch?v=8S1kvCJRfvc	
Unit IV	https://www.youtube.com/watch?v=ntiv1g7G_C4	
	https://www.youtube.com/watch?v=Qe 9CPac23c	
Unit V	https://www.youtube.com/watch?v=4GpWA_hmRhw	
	https://www.youtube.com/watch?v=p4R0Ej6FCn0&list=PLAuW6sm6	dy0yRMXL47Kz4nfhB7tURK88p
	https://www.youtube.com/watch?v=jrQ1YYgiOTo	

		BEC0302			Co	urse Na	<u>me: A</u> 1	nalog C	<u>ircuit</u> s					L	T	P	C
Course	Offere	d in: EE/	VLSI											3	0	0	3
Pre-req	uisite:	Basic kno	wledge o	of Semic	onducto	or device	es.										
Course	Objec	tives:Stud	ents will	l learn a	bout A	C analy	sis of 7	Γransist	ors am	plifiers	, Analys	is and o	design o	f Powe	er and	l Neg	ativ
feedbacl	k ampli	ifiers, App	lications	of Oper	ational .	Amplifi	er, curr	ent miri	ors and	Sinus	oidal & r	non-sinu	ısoidal o	scillato	ors.		
Course	Outco	me: After	completi	ion of the	e course	e, the stu	ıdent w	ill be at	ole to					Bloo Leve		Knowl L)	edg
CO1	Desig	gn and anal	lyze the d	lifferent t	ransistor	amplifi	er circui	ts.									
CO2	Anal	yze the dif	ferent po	ower and	negativ	ve feedb	ack am	plifiers.						К3			
CO3	Design and Explain the applications of Operational amplifier required in electronic systems. Analyze different types of current mirrors used in designing of analog circuits.													K4			
CO4														К3			
CO5	Desig	gn and ana	lyze the	different	t types o	of sinus	oidal an	d non-	sinusoio	dal osci	llators.			K4			
CO-PO	Mapp	ing (Scale	1: Low,	, 2: Med	ium, 3:	High)											
CO-PC Mappi		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO	2	PSO3	
CO1		3	3	2	-	-	-	-	-	-	-	-	1	2		-	
CO2		3	3	3	1	-	-	-	-	-	-	-	2	2		1	
CO3		3	3	3	-	-	-	-	-	-	-	-	2	2		2	
CO4		3	3	2	2	-	-	-	-	-	-	-	3	3		2	
CO5		3	3	3	-	-	-	-	-	-	-	-	3	3		2	
		nts / Sylla															
Module		C Analys														8 hou	
of single	stage	and FET, CE and CS response	S amplifi	ier, low f	requen	cy respo	onse of s	single a	nd mu	ıltistag	current ge e amplif	gain, inp iers. Hig	out resist gh freque	ance, o	utput ansist	resistor mo	del
Module		arge Sign							ac amp	111101.						10 ho	ırs
		er: Variou							ire of m	nerits. r	ower ef	ficiency	and line	arity is			
		back Amp	lifiers: B	lock diag	gram, A												rre
shunt, ef																	

Review of op-amp, Inverting and Non-inverting amplifiers, Voltage follower, Adder, Subtractor, Integrator, Differentiator, Log-Anti Log Amplifiers, Precision rectifier, Comparator, Schmitt trigger.

Active Filters: Frequency response of Low Pass, High Pass, Band Pass, Band Stop, and All Pass Filters, advantages over passive filter. Design guidelines.

Module 4 | Current Mirrors

10 hours

Current Mirrors: Simple current mirror, Base current compensation current mirror, Wilson and Improved Wilson current mirrors, Widlar current source and Cascode current mirror. Design of various stages of operational amplifier.

Module 5 **Oscillators** 10 hours

Sinusoidal oscillators (Op-Amp Based): Concept of positive feedback, Barkhausen criterion, RC oscillators (Phase shift, Wien bridge), LC oscillators (Hartley, Colpitt, Clapp). Non-sinusoidal oscillators: Square wave generator: Astable multivibrator using IC 555, Triangular wave generator.

Total Lecture Hours	48 hours

Textbook:

S.No	Book Title with publication agency & year	Author
1	Design of Analog Circuits, Khanna Publishing House, 2022.	A.V.N. Tilak
2	Microelectronic Circuits, Saunder's College Publishing, Edition IV	A.S. Sedra and K.C. Smith
Refe	rence Books:	
S.No	Book Title with publication agency & year	Author
1	The Art of Electronics, 2nd edition, Cambridge University Press, 1989.	P. Horowitz and W. Hill
2	The Art of Electronics, 2nd edition, Cambridge University Press, 1989.	Paul R.Gray & Robert G.Meyer
3	L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory and applications, McGraw Hill, 1992.	J.V. Wait
NPTEL	/ Youtube/ Faculty Video Link:	
1	https://www.youtube.com/watch?v=2bprLH4cUSo	
2	https://www.youtube.com/watch?v=XDy-rD5AJl0	
3	https://www.youtube.com/watch?v=dHSaPhQIQqE	
4	https://nptel.ac.in/courses/117101106	

Course Code:BEC0306	Course Name: Data Structures	L	T	P	C
Course Offered in: EE/VLSI		2	0	0	2

Pre-requisite: Knowledge of data types and their organization.

Course Objectives:

This course provides an introduction to the principles and processes of microfabrication, with a focus on semiconductor materials and devices. Students will learn about the key steps in microfabrication, such as photolithography, etching, deposition, and diffusion. They will also learn about the properties of semiconductor materials and how they are used to fabricate electronic devices.

Course	Outcome: After completion of the course, the student will be able to	Bloom's Knowledge
		Level (KL)
CO1	Describe how arrays, linked lists, stacks, queues, trees, and graphs are represented in memory, used by the algorithms and their common applications.	K1
CO2	Discuss the computational efficiency of the sorting and searching algorithms.	K2
CO3	Implementation of Trees and Graphs and perform various operations on these data structure.	K4
CO4	Understanding the concept of recursion, application of recursion and its implementation and removal of recursion.	K2
CO5	Identify the alternative implementations of data structures with respect to its performance to solve a real-world problem.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	2	-	3	2	1
CO2	3	3	3	1	2	-	-	-	-	1	-	3	2	1
CO3	3	3	3	2	2	-	-	-	-	1	-	3	3	1
CO4	3	3	2	2	2	-	-	-	-	1	1	3	3	2
CO5	3	3	3	3	2	-	-	-	-	2	1	3	3	2

Course Contents / Syllabus

Module 1 Introduction to data structures, Arrays and Linked Lists

10 hours

Introduction: Basic Terminology, Elementary Data Organization, Built in Data Types in C/python. Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations: Big Oh, Big Theta and Big Omega, Abstract Data Types (ADT) Arrays: Single and Multidimensional Arrays, Representation of Arrays: Row Major Order, and Column Major Order, Index Formulae for 1-D,2-D,3-D and n-D Array Application of arrays, Sparse Matrices and their representations.

Linked lists: Array Implementation of Singly Linked Lists, Doubly Linked List, Circularly Linked List, Operations on a Linked List. Insertion, Deletion, Traversal. Polynomial Representation and Addition Subtraction & Multiplications of Single variable.

Module 2 Stacks and Queues

10 hours

Stacks: Abstract Data Type, Primitive Stack operations: Push & Pop, Array and Linked Implementation of Stack, Application of stack: Prefix and Postfix Expressions, Evaluation of postfix expression, Iteration and Recursion-Principles of recursion, Tail recursion, Removal of recursion Problem solving using iteration and recursion with examples of binary search, Fibonacci numbers, and Hanoi towers. Tradeoffs between iteration and recursion.

Queues: Operations on Queue: Create, Add, Delete, Full and Empty, Circular queues, Dequeue and Priority Queue.

Module 3 Trees 10 hours

Basic terminology used with Tree, Binary Trees, Binary Tree Representation: Array Representation and Pointer (Linked List) Representation, Binary Search Tree, Strictly Binary Tree, Complete Binary Tree, An Extended Binary Trees. Tree Traversal algorithms: In-order, Pre-order and Post-order. Constructing Binary Tree from given Tree Traversal, Operation of Insertion, Deletion, Searching & Modification of data in Binary Search tree,

Introduction of Binary Heaps, Threaded Binary trees, Traversing Threaded Binary trees, AVL Tree, B-Tree.

Module 4 Graphs 10 hours

Graphs: Terminology used with Graph, Data Structure for Graph Representations: Adjacency matrices, Adjacency List. Graph Traversal: Depth First Search and Breadth First Search. Connected Component, Spanning Trees, Minimum Cost Spanning Trees: Prim's and Kruskal's algorithm. Shortest Path algorithms: Dijkstra Algorithm.

Module 5 | Searching, sorting and file structure

8 hours

Searching: Concept of Searching, Sequential search, Index Sequential Search, Binary Search. Concept of Hashing. Sorting: Insertion Sort, Selection, Bubble Sort, Quick Sort, Merge Sort, Heap Sort and Radix Sort. File Structure: Concepts of files, records and files, Sequential, Indexed and Random File. **Total Lecture Hours** 48 hours Textbook: S.No Book Title with publication agency & year Author "Data structures using C and C++", Pearson Education, 2010 Aaron M. Tenenbaum, Yeedidyah Langsam, Moshe J. Augenstein "Data Structures With C", Tata McGraw-Hill Education. 2008 2 Lipschutz **Reference Books:** S.No **Book Title with publication agency & vear** Author 1 "Data Structure using C", OUP Publication. Reema Theraja "Introduction to Algorithms", MIT Press 2 TH Koreman 3 "Programming in ANSI C', Second Edition, Tata McGraw Hill E. Balagurusamy Publication. NPTEL/ Youtube/ Faculty Video Link: Unit 1 https://nptel.ac.in/courses/106/106/106106127/ https://www.youtube.com/watch?v=zWg7U0OEAoE&list=PLBF3763AF2E1C572F https://nptel.ac.in/courses/106/106/106106127/ https://www.youtube.com/watch?v=g1USSZVWDsY&list=PLBF3763AF2E1C572F&index=2 Unit 2 https://nptel.ac.in/courses/106/106/106106127/ https://nptel.ac.in/courses/106/106/106106127/ Unit 3 https://www.youtube.com/watch?v=tORLeHHtazM&list=PLBF3763AF2E1C572F&index=6 https://www.youtube.com/watch?v=eWeqqVpgNPg&list=PLBF3763AF2E1C572F&index=7 Unit 4 https://nptel.ac.in/courses/106/106/106106127/ https://www.youtube.com/watch?v=9zpSs845wf8&list=PLBF3763AF2E1C572F&index=24 https://www.youtube.com/watch?v=hk5rQs7TQ7E&list=PLBF3763AF2E1C572F&index=25 https://www.youtube.com/watch?v=KW0UvOW0XIo&list=PLBF3763AF2E1C572F&index=5 Unit 5 https://www.youtube.com/watch?v=40xBvBXon5w&list=PLBF3763AF2E1C572F&index=22 https://www.youtube.com/watch?v=cR4rxllyiCs&list=PLBF3763AF2E1C572F&index=23 https://www.youtube.com/watch?v=BmayUdDaDYM&list=PLBF3763AF2E1C572F&index=4 https://www.youtube.com/watch?v=KW0UvOW0XIo&list=PLBF3763AF2E1C572F&index=5

Course	Code:	BECVL03	301		Cor	urse Na	me: VI	LSI Tec	hnolog	y				L	T	P	C
Course	Offere	d in: EE-V	VLSI											3	0	0	3
		Basic kno															
	Course Objectives: This course provides an introduction to the principles and processes of microfabrication, with a focus on																
		ductor materials and devices. Students will learn about the key steps in microfabrication, such as photolithography, etching,															
_	eposition, and diffusion. They will also learn about the properties of semiconductor materials and how they are used to fabricate																
Course Outcome. After completion of the course the student will be able to																	
Course													oom's Knowledg vel (KL)				
CO1	Unde	rstand the	basic pr	inciples	of micro	ofabrica	ition.							K 2			
CO2		gn and imp	-											K5			
CO3		acterize se												K4			
CO4		Apply microfabrication techniques to fabricate electronic devices.											K3				
CO5	Know the safety issues involved in the fabrication process. Mapping (Scale 1: Low, 2: Medium, 3: High)											K2					
СО-РО	Mappi	ing (Scale	: 1: Low,	, 2: Med	ium, 3:	High)					1	1	1	1			\neg
CO-PO Mappi		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	P	SO3	
CO1		3	2	-	-	-	-	-	-	-	-	-					
CO2		3	3	-	-	-	-	-	-	-	-	-					
CO3		3	2	-	-	-	-	-	-	-	-	-					
CO4		3	2	-	-	-	-	-	-	-	-	-					
CO5		3	2	2	-	-	-	-	-	-	-	-					
		nts / Sylla															
Module				Enviror												hour	
		or VLSI	Technolo	ogy: Cle	an roor	n and s	safety r	equirem	ents. V	Wafer of	cleaning	proces	ses and	wet ch	emica	al etcl	hing
techniqu Impurity		poration:	Solid St	ate diffi	ision n	nodellin	g and	technolo	ogy. Io	n Imn	lantation	model	lling tea	chnolog	v and	d dan	กลฐล
		acterizatio					S una	Comion	, , 10	p	rantation.	111000	inig, tet	omnorog.	, and	a Guii	ruge
Module	2			Epitaxy	and O	xidatio	n								8	hour	'S
		-Phase Ep wth Kinet															
Module				Lithogr			1	<u> </u>			- I				8	hour	·s
Lithogra	phy: O	ptical Lith				lithogra	aphy, Pl	noto ma	sks, W	et Cher	nical Etc	ching.			- I		
		Polysilicor							on of P	Polysili	con, Sili	con Dio	xide, Sil	icon Ni			
Module				Diffusio											8	hour	S
		els of diff							-		Day C1	D.cc	: T				
		purities in nd Gaseou						-							mant		
Solid, L	iquiu ai	id Gaseou	is source	s. 1011-11	пртанта	iioii. ioii	i-mpiai	itation .	Coming	_l ue, Ka	nge The	ory, mi	giantatio	ii Equip	mem	•	
Module 5 Metal film deposition 8 hours																hour	S
	Metal film deposition: Metallization: Metallization Application, Metallization Choices, Evaporation and sputtering										tion Ch	oices,	Evapora	ation a	nd	sputte	ring
Metal		sical Vanc	techniques, Physical Vapor Deposition, Vacuum Deposition, . Failure mechanisms in metal interconnects; multi-level metallization schemes. CMOS fabrication steps.														
Metal techniqu	es,Phy	_	_		in met	al interc	onnects	; multi-	level m	netalliza	ation sch	emes.C	MOS fa	bricatio	ı step	os.	
Metal techniqu	es,Phy	_	_		in meta	al interc	connects	; multi-	level m	netalliza	ation sch		MOS fa			os. O hou	ırs

S.No	Book Title with publication agency & year	Author								
1	VLSI technology (2nd ed.). New York, NY: McGraw-Hill, (1981).	Sze, S. M.								
2	Fundamentals of microfabrication (2nd ed.). Boca Raton,FL: CRC	Madou, M. J.								
	Press,(2002)									
Ref	erence Books:									
S.No	Book Title with publication agency & year	Author								
1	Introduction to microelectronic fabrication (2nd ed.).Upper Saddle River,	Jaeger, R. C.								
	NJ: Prentice Hall.(2002).									
2	Physics of semiconductor devices (3rd ed.).Hoboken, NJ: Wiley. (2006).	Sze, S. M., & Kwok, K. N.								
NPTEI	Youtube/ Faculty Video Link:									
1	https://archive.nptel.ac.in/noc/courses/noc15/SEM1/noc15-ec02/									
2		https://video.search.yahoo.com/search/video; ylt=AwrjbCfLAhtoPicCgpRXNyoA; ylu=Y29sbwNncTEEcG9zAzEE								
	dnRpZAMEc2VjA3BpdnM-?p=VLSI+Technology&fr2=piv-									
	web&type=E210US826G0&fr=mcafee#id=7&vid=5e694387d34857a70									
3	https://video.search.yahoo.com/search/video; ylt=AwrjbCfLAhtoPicCg	pRXNyoA; ylu=Y29sbwNncTEEcG9zAzEE								
	dnRpZAMEc2VjA3BpdnM-?p=VLSI+Technology&fr2=piv-									
	web&type=E210US826G0&fr=mcafee#id=15&vid=5fa3bdf0373ac3724	4665542bdfb6fb3d&action=view								
4	https://nptel.ac.in/courses/117101106									

LAB Course Code: BEC0351	LAB Course Name: Digital System Design Lab	L	T	P	С
Course Offered in: EE/VLSI	0	0	4	2	
Due magnista. Desire server of saidless	tic counting Design of designal number systems				

Pre-requisite: Basics concept of arithmetic operations, Basic of decimal number system.

Course Objectives: The student will learn about

1.	Verification of truth table of various type of logic gates.	K2
2.	Designing and verification of different type of combinational circuits.	K4
3.	Implementation and verification of truth table of various type of flip-flops.	K3
4.	Designing and implementation of different types of sequential circuits.	K4

Course	Course Outcome: After completion of the course, the student will be able to Bloom's Knowledge							
		Level (KL)						
CO1	Verify truth table of various type of Logic Gates.	K2						
CO2	Design, implement and verify combinational logic circuits.	K4						
CO3	Implement and verify truth table of various types of flip-flops.	K3						
CO4	Design and analyse different types of sequential logic circuits.	K4						

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	-	-	-	-	-	3	2	2	-	1	2	2
CO2	3	3	3	-	-	-	-	3	2	2	-	1	2	2
CO3	3	2	3	-	-	-	-	3	2	2	-	1	2	2
CO4	3	3	3	-	-	-	-	3	2	2	-	1	2	2

List Of Practical's (Indicative & Not Limited To)

- 1. Verification of the truth tables of Basic Logic Gates and Universal Logic Gates using TTL ICs.
- a) AND (7408)
- b) OR (7432)
- c) NOT (7404)
- d) NAND (7400)
- e) NOR (7402)
- 2. Implementation of the given Boolean function using TTL Logic Gates (NOT, AND and OR Gates) in SOP for following Boolean expressions:
- a) Y1 = AB' + A'B
- b) Y2 = ABC + A'B'C' + A'C
- c) $F(A,B,C,D)=\sum (0,2,5,7,8,10,13,15)$
- 3. Implementation of the given Boolean function using TTL Logic Gates (NOT, AND and OR Gates) in POS forms for following Boolean expressions:
- a) Y1 = (A'+B)(A+B')
- b) Y2 = (A+B+C)(A'+B'+C')(A'+C)
- c) F(A,B,C,D) = M(0,2,5,7,8,10,12,15)
- 4. Implement and verify
- 4-bit Binary to Gray code converter and
- 4- bit Gray to Binary code converter.
- 5. Implementation of Half-adder, Full-adder and Full-adder using two Half-adder with TTL Logic Gates (EXOR-7486, AND-7408, OR-7432) and verify its truth table.
- 6. Implementation of Half-subtractor, Full-subtractor and Full-subtractor using two Half-subtractor with TTL Logic Gates (EXOR-7486, AND-7408, OR-7432) and verify its truth table.
- 7. Implementation of 4-bit Parallel adder using 7483 IC and verify the outputfor the given inputs.
 - (i) A = 1011, B = 1001

- (ii) (ii) A = 0011, B = 0010
- 8. Implementation of 2:4 Decoder, 1:4 Demultiplexer using Logic Gates (NOT gate- 7404, AND gate- 7408) and verify its truth table
- 9. Implementation of 4:2 Encoder, 4:1 multiplexer using logic gate (OR gate-7432) and verify its truth table.
- 10. Implement and verify $F(A,B,C) = \sum (3, 5, 6, 7)$ using
 - a) 8:1 multiplexer.
 - b) 4:1 multiplexer.
- 11. Implement 2 Bit magnitude comparator using logic gates and verify the truthtable.
- 12. Verification of truth table of flip-flop using NAND gate (7400) & NOR gates (7402).
 - a) RS Flip Flop
 - b) JK Flip Flop
 - c) D Flip Flop
 - d) T Flip Flop
- 13. Implement D flip flop using SR flip flop and verify the truth table.
- 14. Design and implement 4-bit ring counter using D flip flop and verify the result.
- 15. Design MOD 5 asynchronous counter using T flip flop and verify the truth table.
- 16. Design MOD 5 synchronous counter using T flip flop and verify the truth table.
- 17. Realize
 - a) Design Mod N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop
 - b) Mod-N Counter using IC7490 / 7476
 - c) Synchronous counter using IC74192
- 18. Design Pseudo Random Sequence generator using 7495.

Total Hours: 48 hrs.

LA	B Co	urse C	ode: BEC0352	LAB Course Name: Analog Circuits Lab	L	T	P	C			
		0.00	1 • PP/V/ CI		_		_	_			
_			d in: EE/VLSI		0	0	4	2			
Pre	Pre-requisite: The operation and characteristics of semiconductor devices.										
Cor	urse (Objecti	ives: Students will learn abou	t							
	1.		Designing, implementation	and verification of various characteristics of transistor amplifiers.	s. K5						
	2.		Design and implementation	of various applications of Op-amp.	K5						
	3.	. Design and implementation of oscillators.									
	4.		Simulation of Electronic cir	cuits on simulation software.	K4						
	5.		Introduction and circuit des	ign by PCB design software (PCB Express, Ki cad).							
Cor	urse (Outcon	ne: After completion of the co	ourse, the student will be able to	Bloc	Bloom's Knowledge					
					Leve	el (KL	ر)				
CO)1	Desig	n and plot frequency response	e of amplifiers.		k	3				
CO)2	Desig	n and verify Op-amp base cir	cuits.		k	C 3				
CO)3	Desig	n and verify of oscillator circ	uits.		k	K 3				
CO)4	Simulate the Electronic circuits on simulation software. K3									

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-I O Map	ping (Bear	C II LOW	,	14111, 01	6/	,								,
CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	1		2	2	-	2	2	2	-	1	2	2
CO2	3	3	2		3	2	-	2	2	2	-	1	2	2
CO3	3	3	2		2	2	-	2	2	2	-	1	2	2
CO4	3	3	2		3	2	-	2	2	2	-	1	2	2
CO5	3	3	3		2	2	-	2	2	2	-	1	2	2

K3

Design and implement electronics circuits by PCB design software (PCB Express, Ki cad).

List Of Practical's (Indicative & Not Limited To)

- 1. Design and implement a CE (BC-107) amplifier with potential divider biasing (for V_i = 20 mV, R_1 =100K Ω R_2 = 10K Ω , R_C = 4.7 K Ω , R_E = 1K Ω). Verify the following parameters with the theoretical values:
 - (i) Voltage gain A_v
 - (ii) Current gain Ai
 - (iii) Input Resistance (Ri)

Output Resistance (R_o)

- 2. Design and analysis of Single stage common source MOSFET amplifier with potential divider biasing (for $V_i = 20$ mV, $R_1 = 1M\Omega$ $R_2 = 1K\Omega$, $R_D = 4.7$ K Ω , $R_S = 1K\Omega$) and Plot Gain (dB) Vs frequency curve, also measure following parameters
- (i) Bandwidth
- (ii) Input impedance

Maximum signal handling capacity (MSHC).

- 3. Design a single-stage CE and a multistage (CE-CE) amplifiers with Voltage Divider Bias for 10 mV input ac signal and plot the Frequency Response curves using BC 547, $V_{CC}=12V$, Stability factor (S) =10 and $R_L=10~K\Omega$. Observe the effect on gain and bandwidth.
- 4. Design current series/Voltage shunt Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain, bandwidth input and output impedance.
- 5. Design Voltage series Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain, bandwidth, input and output impedance.
- 6. Design and analyze the output voltage V_0 for OP-AMP (IC 741) as:
 - (i) Inverting and Non-inverting amplifier for input voltage 0.5V with input Resistance (R_i) of 10 K Ω and feedback Resistance (R_f) of 100 K Ω .
 - (ii) Voltage follower circuits for input voltage 1V.

- 7. Design a differential amplifier with $\pm 12V$ DC power supply and calculate Common mode gain, differential mode gain, CMRR and slew-rate.
- 8. Design and analyze OP-AMP applications as a difference amplifier, integrator and differentiator Circuits for 1 KHz input signal.
- 9. Draw the input and output waveforms of a given full wave precision rectifier.
- 10. Design and implment of 2nd order Active Low pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify cutoff frequency.
- 11. Design and implement of 2nd order Active High pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.
- 12. Design the following RC sinusoidal oscillators; Also verify the theoretical and practical Oscillating frequency.
- (i) RC phase shift oscillator, if its frequency of oscillation is 955 Hz and $R_1=R_2=R_3=680$ K Ω .

Wien bridge oscillator uses R=4.7K Ω , C=0.01 μ F, and R_F=2R₁

- 13. Design the following LC oscillators; Also verify the theoretical and practical Oscillating frequency.
- (i) For a Hartley oscillator, self-inductance of the two coils are $L_1=100$ mH, $L_2=1$ mH and mutual inductance between the two coils is 20μ H. its output for a capacitor of value 20pF.

For a Colpitts oscillator in which feedback network consists of two capacitors of 100 pF and 20 pF with 100 mH coil across these capacitors.

- 14. Design and implement square wave generator (Astable Multivibrator) for 1 KHz using,
 - (i) Op-amp
 - (ii) IC 555.
- 15. Design and implement a triangular wave generator using dual op-amp, for oscillation frequency f_0 =1.5 KHz and Vout (P-P) =6V, use Vsat = 13.5 V.
- 16. Design and simulate single-stage CE amplifiers with Voltage Divider Bias for 10mV input ac signal and plot the Frequency Response curves using BC 547, V_{CC} = 12V, Stability factor (S)=10 and R_L = 10 K Ω . (TARGET, PSPICE-1etc.)
- 17. Simulation of Multistage stage (CE-CE) amplifier (designed in experiment1) using any available simulation software and also find the Voltage gain, Input impedance, Output impedance, and bandwidth. (*TARGET*, *PSPICE-1*etc.)
- 18. Design and simulate current series/Voltage shunt Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain and bandwidth.
- 19. Design and simulate Voltage series Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain and bandwidth.
- 20. Design and simulate of 2nd order Active Low pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.
- 21. Design and simulate of 2nd order Active High pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.
- 22. Introduction of PCB design software (PCB Express, Ki cad).
- 23. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.
- 24. PCB Lab: Artwork & printing of a simple PCB.
- 25. Etching & drilling of PCB.
- 26. Wiring & fitting shop: Fitting of power supply along with a meter in cabinet.
- 27. Mini Project: Design a mini project using the applications of this Lab.

Total Hours: 48 hrs.

LAB Co	urse Co	ode: BEC	0356		LA	B Cour	se Nam	e: Data	Struc	ture L	ab			L	T	P	C		
Course (Offered	l in: EE-V	/LSI											0	0	2	1		
		Basic know		f prograi	nming	concept	s using	C/C++	and un	derstan	ding of	fundam	ental algo	orithms	_				
Course (Objecti	ves:																	
		ises on the	basic co	oncepts o	f algori	thm ana	alysis, al	long wi	th impl	ementa	tion of l	inear an	d non-lir	near dat	a st	ructure	s and		
file struc	tures.																		
Course	Outcom	ne: After o	completi	on of the	course	the stu	dent wi	ll be ab	le to					Bloom	m's	Knowl	ledge		
			1											Leve			υ		
CO1	Imple	menting S	ingle an	d Multi-	dimensi	onal ar	ray with	their a	pplicati	ons lik	e search	ing and	Sorting			K3			
	techni		11 . 0.	1 10		1.1 .1													
CO2		ment Link mentation							ka insa	artion	deletion	coarch	ing and			K3			
CO3	traver		or nee	uata sirt	ictures	ioi bas.	ic opera	mons n	KC IIISC	ruon,	deletion,	, scarcii	ing and			K4			
CO4		mentation			various	operati	on like	searchi	ng, sort	ing, ha	shing in	data sti	ructures			K4			
	for so	lving real	world pi	oblems.												174			
CO-PO	Mannii	ng (Scale	1 · I ow	2. Medi	um 3.	High)													
СО-РО	\							_											
Mappir	l II	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO	2	PSO3	1		
GO1		3	2	3	2	3	_	_	_	_	2	_	3		3		1		
CO1																			
COA		3	3	3	2	3	-	-	-	-	1	-	3		3		1		
CO2																			
CO3		3	3	3	2	3	-	-	-	-	1	-	3		3		1		
COS																			
CO4		3	3	3	3	3	-	-	-	-	2	1	3		3		2		
List Of l	Practica	al's (Indic	cative &	Not Lir	nited T	0)													
S. No.	Des	scription														CO			
1	Co	nstruct a	code to	find the	maxir	num el	ement	in an a	rray.							CO	1		
2	Co	nstruct a	code to	calcula	te the s	um of	all elen	nents in	n an ar	ray.						CO	l		
3	Co	nstruct a	code to	reverse	the ele	ements	of an a	rray.								CO	1		
4	Co	nstruct a	code to	count t	he occi	ırrence	of a sp	pecific	elemer	nt in a	n array.					CO	1		
5		nstruct a										olumn	major o	rder.		CO	l		
6	Pro	gram to	find if a	given 1	natrix	is spars	se or no	ot and p	rint sp	arse n	natrix.					CO	l		
7	Co	nstruct a	code to	represe	nt a sp	arse ma	atrix in	triplet	form.							CO	1		
8		nstruct a								ecursio	on.					CO2	2		
9		nstruct a														CO2	2		
10		nstruct a														CO2			
11		nstruct a				_										CO2			
12		nstruct a				_		•								CO2			
13		nstruct a														CO2			
14		eate a sin				_			s (inse	rtion.	deletion	. traver	sal).			CO2			
15		eate a doi														CO2			
16		eate a circ														CO2			
17		ite a prog						_								CO2			
1 /	VVI	ne a pros	grain to	mpiem	em an	111-01 U	n nave	18a1 UI	a villa	ту пее	and pri	ini ine l	ioues.				,		

18	Write a program to implement a pre-order traversal of a binary tree and print the nodes.	CO3
19	Write a program to implement a post-order traversal of a binary tree and print the nodes.	CO3
20	Write a program to count number of nodes in a binary tree.	CO3
21	Write a program to find the height of the tree.	CO3
22	Write a Program to search a number in Binary Search Tree (BST).	CO3
23	Write a program to insert a node in a Binary Search Tree (BST).	CO3
24	Write a program to delete a node from a Binary Search Tree (BST).	CO3
25	Write a program to implement Prims Algorithm.	CO4
26	Write a program to implement Kruskal Algorithm.	CO4
27	Write a program to implement Dijkstra Algorithm.	CO4
28	Write a program to perform Depth-First Search (DFS) on a graph.	CO4
29	Write a program to perform Breadth-First Search (BFS) on a graph.	CO4
30	Construct a program to implement merge sort with recursion and iteration.	CO4
31	Construct a program to implement quick sort with recursion and iteration.	CO4
32	Construct a code to implement linear search.	CO4
33	Construct a code to implement binary search.	CO4
34	Construct a program to implement bubble sort.	CO4
35	Write a program to implement a max-heap and perform heap sort on an array of integers.	CO4
	To	tal Hours: 48 hrs.

LAB Co	ourse Co	ode: BE0	CVL035	5	LA	B Cour	se Nan	ne: Linu	ux and	Script	ing			L	T	P	(
Course	Offered	in: EE-	VLSI											0	0	6		
Pre-req	uisite: B	Basis con	cept of o	perating	system.													
Course	Objecti	ves: The	student	will lear	n about													
		e the bas																
		essential							nux con	nmands	S.							
		basic scr																
		nux and													1		_	
Course	Outcom	e: After	comple	etion of	the cou	rse, the	studei	nt will	be able	e to					loor			
																edge		
														Le	vel ((KL)	_	
CO1	Under	stand Lir	nux basic	s, direct	ory stru	cture, ai	nd esser	ntial cor	nmand-	line ut	ilities.				K2	2		
CO2	Apply	Linux co	ommand	s for file	handlin	g, syste	m moni	toring,	and dis	k mana	gement.			К3				
CO3	Develo	op and ex	xecute To	CL scrip	ts for au	tomatic	n and b	asic sys	stem tas	ks.				К3				
CO4	Analyz	ze and di	fferentia	te Linux	comma	nds and	TCL s	cripts to	solve	admini	strative p	oroblem	s.	K4				
СО-РО	Mappin	ng (Scale	1: Low,	, 2: Med	ium, 3:	High)												
CO-PO Mappii		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	2]	PSO3	,	
CO1		3	2	-	-	3	-	-	-	-	2	3	3	2		2		
CO2		3	3	-	3	3	-	-	-	-	2	3	3	2		2		
		3	3	_	3	3	-	-	-	3	2	3	3	2		2		
CO3		3	5														_	

Course Contents/Sy	llabus	
Module 1	Introduction to Linux for VLSI Design	8 hours
Overview of Linux d	istributions and their relevance in VLSI design. Basic Linux commands and file system is	navigation
Module 2	Advanced Linux Commands for VLSI Design	8 hours
Networking and syste	em administration in a VLSI design environment. Version control systems for collaborati	ive VLSI projects.
Module 3	Introduction to Python Programming for VLSI	8 hours
Basic Python syntax	and data structures. Writing and executing Python scripts for VLSI design automation.	
Module 4	Introduction to TCL Scripting for VLSI	8 hours
TCL fundamentals ar	nd scripting in VLSI applications, Integrating TCL with EDA tools for automation.	
Module 5	Advanced TCL Scripting for VLSI Design	8 Hours
Developing complex	TCL scripts for VLSI design tasks. Interfacing TCL with Python for enhanced functional	lity.

S.No	Book Title	Author
1	Practical Programming in TCL and TK	Jones, Ken, Welch, Brent
2	Linux Commands for Beginners	Khalid Husain
G.N.	D 1 mg to 11 to 0	1.4.0
S.No	Book Title with publication agency & year	Author Payon Kumar Nalluri
S.No	Book Title with publication agency & year Commands Of Kali Linux: Commands	Author Pavan Kumar Nalluri
S.No 1 2	1 0 1 1	

1. Linux Programming and Scripting, IIT Madras, Prof. Indranil Sengupta

 $\underline{https://archive.nptel.ac.in/courses/117/106/117106113/}$

2. C-DAC (PG-DVLSI)

https://www.cdac.in/index.aspx?id=DVLSI&courseid=20

3. Linux for Beginners, Infosys Springboard

TOC - Linux for Beginners | Infosys Springboard

Links:

 $\underline{https://www.youtube.com/watch?v=ZRi2VHoS8qE\&list=PL1h5a0eaDD3rsGDFnVki_fFEtDWQfXjca\&index=2}$

 $\underline{https://www.youtube.com/watch?v=SI4_zKTmKdk\&list=PL1h5a0eaDD3rsGDFnVki_fFEtDWQfXjca\&index=4}$

https://www.youtube.com/watch?v=J7SLbhZv08c&list=PL1h5a0eaDD3rsGDFnVki fFEtDWQfXjca&index=5

3. To implement	and execute Linux Directory Structure.	CO1
 To implement To implement 	and execute Linux Directory Structure.	
3. To implement	•	CO1
-	and an anta Linna Davis Commands	COI
4. To implement	and execute Linux Basic Commands.	CO1
	and execute Copy, Remove, Move and Time Commands.	CO1
5. To implement	and execute df, diff and Grep Commands and differentiate between df and diff commands.	CO1
6. To implement	and execute Head, tail, sort and more commands.	CO1
7. To implement	and execute tr and wc commands.	CO1
8. To Study Getti	ng Help From Command Line user Interface (CLI).	CO1
9. To implement	and execute rmdir and exit command.	CO1
10. To implement	and execute date and more command.	CO2
11. To implement command.	and execute cat, less and more command and explain the difference between cat and less	CO2
12. To implement	and execute sort, scp command.	CO2
13. To implement	and execute Disk utilities like fdisk, df and du commands.	CO2
14. To implement	and execute w, who, hostnamem hostnamectl and uname commands.	CO2
15. To implement	and execute Search for files and directories using find and locate commands	CO2
16. To implement	and execute top command and its output explanation	CO2
Part II - TCL	Scripting experiments	
17. To Write Exan	nple TCL script that takes a user's name as input and greets them.	CO3
18. To Write Exan	nple TCL script that do	CO3
1. String	Comparison	
2. Index	creation	
3. Calcu	lation of Length of String	

20. To Write Example TCL script that creates	CO3
1. Trimming of Characters.	
2. Identification of Matching Strings.	
21. To Write Example TCL script demonstrating Append Command	CO3
1. List Creation.	
2. Appending Item to a List	
3. Length of List	
22. To Write Example TCL script that calculates the sum of integers from 1 to N using a loop.	CO4
23. To Write Example TCL script that searches for a specific word in a file and counts its occurrences.	CO4
24. To Write Example TCL script to illustrate 'for' loop.	CO4
25. To Write Example TCL script to illustrate Arithmetic operators.	CO4
26. To Write Example TCL script to display the structure of your file system directory.	CO4
27. To Write Example TCL script to modify all files in a directory.	CO4
28. To Write Example TCL script to Take Backup of a Particular File.	CO4
29. To Write Example TCL script to Connect to remote host and send the password (create automate login SSH).	CO4
30. To Write Example TCL script to Collect Multiple Servers CPU, MEM, DISK usage in single report.	CO4
Tota	l Hours: 60 hrs.

Course C					C	Course N	ame: A	Artificia	l Intellg	ence and	l Cyber E	thics	L	T	P	C
Course O													2	0	0	2
Pre-requi																
Course O	-							_				_				у,
										Artificia	l Intellige	nce and				
Course O	utcome:	After c	omplet	ion of t	he cour	se, the st	udent v	will be a	able to							ledge
														el (KL	ر)	
	Learn ke developn		-		ethics,	summari	izing e	thical o	considera	ations an	d applicat	ions in A	AI	K	(2	
	Apply po													K	3	
	Apply prand Cybe	-		rity co	ncepts,	risk man	ageme	nt and r	egulator	y complia	ance in the	field of	AI	K	3	
CO4		nd the	nature							property	rights (IP	R), and t	he	k	(2	
CO-PO N													.			
СО-РО	DO1	DO.	DO2	DO 4	DO.	DO.	DO#	DOG	DOG	DO10	DO11	DGO1	DG 0.2	DO	22	
Mapping	g PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSC)3	
CO1	_	1	-	-	-	1	2	-	-	-	2	1	1	1		
CO2	2	3	2	-	2	1	2	-	2	1	2	2	1	1		
CO3	2	3	2	1	2	3	3	-	2	2	2	2	2	1		
CO4	2	2	-	-	1	3	3	-	2	2	2	2	1	1		
Course C	ontents /	Syllab	us							•		•				
Module 1	-			An Ov	erview	to AI E	thics							(6 hou	ırs
Definition	of AI Etl	hical pr	inciple	s in AI,	Source	s of AI d	lata, Le	gal imp	lications	of AI Se	curity Bre	aches, Pri	ivacy and	AI R	egula	tions,
Key Princ	ciples of	Respon	sible A	I, Tran	sparen	cy and A	Accoun	tability,	Dual-U	se Dilem	ma, Huma	an-Centri	c Design	, Intro	ducti	ion to
Cyber Lav	ws and Et	hics, H	istorica	l Devel	opmen	t of Cybe	er laws,	Legal	framewo	rks.						
Module 2	2			Fairne	ess and	Favoriti	ism in	Machir	ne Learn	ing				:	8 hou	ırs
											d Fairness					
Fairness a										neworks	for Fairne	ss in AI,	Bias in	Data (Colle	ction,
Fairness in Module 3		ocessiii	g, Gene			d Cybers								Τ,	8 hou	ırs
		acv and	Securi						_	are Prive	acy-Preser	ving Mac	hine I ea			
											Incident R					
											in engine				1	
Module 4	ļ			Cyber	crimes	, IPR an	d Lega	l Meas	ures						8 hou	ırs
* -	•			-	_						d Prosecut					
Patents, ar																
											endments),	Compara	ative Ove	rview	: Indi	ian vs
Global Cy	ber Laws	, Case	Study:	The AT	M Hei	st – Cosr	nos Ba	nk Cyb	er Attack	(India, 2	-	5 4 1 T			20.1	
Tor-4L 1											']	Total Lec	ture Hou	irs .	30 ho	ours
Textbook S.No	<u> </u>	Boo	ok Title	e with p	oublica	tion age	ncy &	year				Auth	or			
1.	Artifici	al Intel	ligence	: A Gui	de for	Thinking	Huma	ns by P	enguin	M	Ielanie Mit	tchell				
	Books,		8						- 6							
2.	•	Ethics:	Moralit	y and I	nd Law in Cyberspace, 7th Edition (2023) Richard Spinello, Jos							nello, Jor	ies & Bai	tlett L	earni	ing
Reference	e Books:	-								<u> </u>						
S.No		Boo	ok Title	e with p	publica	tion age	ncy &	year		A	uthor					
1.	Artifici	al Intel	ligence	and Et	hics by	, BPB Pu	ıblicatio	ons, 202	23.	S.	B. Kishor	, Debajit	Biswas			
2.	Cyber S	Security	y and C	yber La	aws by,	Cengage	e India,	2022.		A	lfred Basta	a, Nadine	Basta, S	attwik	Pand	la

NPTEL/ Yo	uTube/ Faculty Video Link:
1.	https://www.youtube.com/watch?v=VqFqWIqOB1g
2.	https://www.youtube.com/watch?v=hVJqHgqF59A
3.	https://www.youtube.com/watch?v=O5RX T4Tg24
4.	https://www.youtube.com/watch?v=RJZ0pxcZsSQ

Course Code	e: BASC	C0401			Co	ourse N	ame: E	Employ	ability	Skill D	evelopn	nent - II	L	T	P	\mathbf{C}	
Course Offer	red in: B	.Tech			•								2	0	0	2	
Pre-requisite	e: Basic u	ındersta	anding o	of eleme	entary 1	nathem	atics										
Course Obje	ectives:																
The objective				-		-	-		_		_	-	-			-	
puzzles, and l	ousiness r	nathem	atics, e	nabling	them to	solve i	real-wo	rld and	compet	titive ex	am prob	lems with	speed, a	ccuracy	, and lo	ogica	
thinking.													1				
Course Outo	come: Af	ter com	pletion	of the o	course,	the stud	dent wil	l be ab	le to				Bloom Level	n's Kno (KL)	wledge	3	
CO1	theorei	m, and	cyclicit	y to sol	ve quar	ntitative	proble	ms effi	ciently.			emainder		K2,	K3		
CO2	sense,	blood r	elations	s, series	pattern	s, and t	time-ba	sed puz	zles lik	e clock	s and ca			K	3		
CO3	interes	t averag	ge calcu	ılations	and us	sing app	propriat	e mathe	matica	l metho	ds	liscounts,	K2, K3				
CO4	Solve real-life business math problems involving averages, mixtures, and ratios us appropriate mathematical methods O-PO Mapping (Scale 1: Low, 2: Medium, 3: High)													K2,	K3		
CO-PO Map	oping (Sc	ale 1: I	∠ow, 2:	Mediu	m, 3: I	ligh)	ı		I	ı	1	1		1	-		
СО-РО Ма	CO-PO Mapping PO1 PO2 1					PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PS	502	
CO1		1	1	1	1	-	-	-	-	-	-	-	-	-		-	
CO2		1	1	1	1	-	-	-	-	-	-	-	-	-		-	
CO3		1	1	1	1	-	-	-	-	-	-	-	-	-		-	
CO4		1	1	1	1	-	=.	-	-	-	-	-	-	-		-	
Course Cont	tents / Sy	llabus							1		ı			1			
Module 1				Spee	d Matl	and N	lumber	Syster	n						8 hou	irs	
Classificatior Remainder th				•					I, It's A	Applica	tion, Mo	dule digi	t(Cyclici	ty), Las	st two	digi	
Module 2				Anal	ytical a	and Lo	gical R	easonii	ng						8 hou	ırs	
Direction and	l Sense, I	Blood R	elation	, Numb	er Serie	es and I	Letter S	eries, C	oding I	Decodir	ng,						
Module 3				Busin	ness M	ath I									8 hou	irs	
Percentage, P	Profit and	Loss, I	Discoun				Compo	ound In	terest, A	Average)						
Module 4					ness M										8 hou	irs	
Ratio & Prop	ortion, Pa	artnersh	11p, M13	ture &	Allega	tion, Cl	ock, C	alendar				Total I	Lecture 1	Loung	32 ho		
Refe	erence Bo	ooks:										1 otal 1	zecture i	TOUTS	<i>34</i> H0	urs	
											ı						
S.No		k Title									Aut						
1	_ `	cker ma										Γyra (BSC	c publica	tion co.	Pvt. I	Ltd)	
2		ıntitativ										Aggarwal					
3	Ver	bal & N	Von-Ve	rbal Rea	asoning	Ţ					RS .	Aggarwal					

Sarvesh K Verma

Quantitative Aptitude - Quantum CAT

4

Course	Code:	BECVL0	401		Co	urse Na	me: Aı	nalog a	nd Digi	tal Sig	nal Pro	cessing	&	L	T	P	С
					Co	mmuni	cation										
		d in: VLS		6 : .	1									3	0	0	3
		Basic Kn				. C 1	Ľ4 1	. 1 1.4	(A B :	f) 1	1	1.1.4.	1 1.	1 1	··	4 1	
	-	ives: This tion. Fur				-					_						-
		e perform			-				_						-		
		protocol													ері (JI UIII	CICII
		ne: After								mergin	g comm	umeano	ii teeiiile	Bloom	n's I	Znowl	eda
Course	Outcol	nc. 7 mer	complet	ion or th	c course	, the ste	adent w	iii oc ac	10 10					Level			cug
	Τ													Level	(111		
CO1	Expla	in the fui	ndamenta	ıls of sig	nal and	systems	s with si	gnal pr	ocessin	g.				K2			
CO2	Desig	gn of digit	tal IIR an	d FIR fi	lters.												
CO2														K5			
CO3		in variou	s modula	ition and	demod	ulation	method	s of Am	plitude	Modu	lation an	d Angle	;	K4			
		ılation.												IX-T			
CO4	Expla	ain variou		K3													
GO.	Explain different communication protocols and various emerging communication technologies																
CO5														K1			
СО-РО	Mappi	ing (Scale	e 1: Low	, 2: Med	ium, 3:	High)	1			T	•	1					
CO-PC	O-PO Mapping (Scale 1: Low, 2: Mo				DO 4	DO 5	DOC	DO#	DOG	DOG	DO10	DO11	DGO1	DGOA	.	DG O A	
Mappi	ng	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	'	PSO3	
CO1		3	3	2	<u> </u>	_	_	<u> </u>	_	<u> </u>	_	2	3	2		2	_
CO2		3	3	3	_	_	_	<u> </u>	_	_	_	2	3	2		2	=
CO3		3	3	2				 	<u> </u>			2	3			2	_
				+	-	-	-	+ -	-	-	-			2			
CO4		3	3	2	-	-	-	-	-	-	-	2	3	2		2	
CO5		3	3	3	-	-	-	-	-	-	-	2	3	2		2	
		ts / Sylla	bus														
Module				Signal (cessing					8 hou	rs
		of Signals					ne-reve	rsal pro	perties.								
		of system ing: ASP					ition Li	near fil	terino 11	sing ci	rcular co	nvolutio	on Fast F	ourier t	rans	form:	DIT
_		FT algori		, 11, 0	on Curur	Convoid	ition, Li	iicui iii	tering a	Sing Ci	ediai co	ii v Oiutiv	on r ust r	ourier t	i uii o	ioiiii.	D11
Module	2	-		Digital	Filter D	esign:	IIR and	I FIR T	echniq	ues						8 hou	rs
IIR filte	r: Filte	r transfor	mation: i	impulse	invarian	t and B	i linear	transfo	mation	metho	d, All po	le filter	, Freque	ncy Trai	nsfo	rmatic	n
		quency re	sponse o									es and v	vindow t	echniqu			
Module				Fundan						•						8 hou	
		Commu									ation an	d Dem	odulatio	n, Angl	e N	Iodula	tion
Frequen Module		lulation a	nd Demo	Digital							,					8 hou	re
		orem, Pul	lse Code							_		PSK M	Iodulatic	n and			
	_	ise shift k			•			•			i Six &	I SIX IV	iodulatic	ni and	DCII	iouuii	шоп
الالالالالالا	mu piic	.se siiit K	cymg (D	, Q	uuuratu	re pirast	omit K	cymg (ζι DIX).								
Module	5			Commu	ınicatio	n Proto	ocols an	d Eme	rging T	echno!	logies					8 hou	rs
Introduc	ction to	Commun	ication P									s, Protoc	col stand	ards and			
muoduc										, 44		, - 5000			ع ح		
		ΓU), Basi	c Comm	unicatior	Protoc	ols: IP,	UDP, T	CP, Ap		n Leve		unicatio	n Protoc	cols: FT	P, T	ELNE	ΞT,

Emerging Communication Technologies: Internet of Things (IoT): Protocols – MQTT, CoAP, 6LoWPAN, Industrial IoT (IIoT): Modbus, CAN, OPC UA, Edge and Fog Computing in communication, Low-Power Wide Area Networks (LPWAN): LoRaWAN, NB-IoT

		Total Lecture Hours 40 hours								
Textboo	k:	,								
S.No	Book Title with publication agency & year	Author								
1	John G Prokias, Dimitris G Manolakis, "Digital signal processing Principles	John G Prokias, Dimitris G Manolakis								
	Algorithms & Applications", 4th edition, Pearson education, 2007.									
2	Herbert Taub and Donald L. Schilling, "Principles of Communication	Herbert Taub and Donald L. Schilling								
	Systems", Tata McGraw Hill									
3	B.P. Lathi, "Modern Digital and Analog communication Systems", 4th	B.P. Lathi,								
	Edition, Oxford University Press,2010.									
4	Behrouz A. Forouzan, "Data Communications and Networking", 5 th	Behrouz A. Forouzan								
	Edition, McGraw- Hill									
Referen	ce Books:									
G NI		Las								
S.No	Book Title with publication agency & year	Author								
1	Simon Haykin, "Communication Systems", 4th Edition, Wiley, India	Simon Haykin								
2	H.P.Hsu & D. Mitra "Analog and Digital Communications", 2nd Edition,	H.P.Hsu & D. Mitra								
	Tata McGraw- Hill.									
3	Oppenheim & Schafer, "Discrete Time Signal Processing", Pearson	Oppenheim & Schafer								
	education, Prentice Hall, 2nd edition,2003									
NPTEI	Youtube/ Faculty Video Link:									
1	https://archive.nptel.ac.in/noc/courses/noc15/SEM1/noc15-ec02/									
2	https://video.search.yahoo.com/search/video;_ylt=AwrjbCfLAhtoPicCgpRXNyoA;_ylu=Y29sbwNncTEEc0									
	dnRpZAMEc2VjA3BpdnM-?p=VLSI+Technology&fr2=piv-									
	web&type=E210US826G0&fr=mcafee#id=7&vid=5e694387d34857a70efe44d25f2595c7&action=view									
3	https://video.search.yahoo.com/search/video; ylt=AwrjbCfLAhtoPicCgpl	RXNyoA; ylu=Y29sbwNncTEEcG9zAzEE								
	dnRpZAMEc2VjA3BpdnM-?p=VLSI+Technology&fr2=piv-									
	web&type=E210US826G0&fr=mcafee#id=15&vid=5fa3bdf0373ac37246	US826G0&fr=mcafee#id=15&vid=5fa3bdf0373ac3724665542bdfb6fb3d&action=view								
4	https://nptel.ac.in/courses/117101106									

Course Cod	e: BECVL0	402			Cours	e Nam	e: CMO	OS Ana	alog In	tegrated	l Circui	it		L	T	P	1
Course Offe	ered in: VLS	I												3	0	0	
Pre-requisit	e:: Basic ur	derstand	ling of e	lectroni	c device	es, circu	it theor	y, and	operatio	onal amp	olifiers. l	Familiar	ity wit	th SP	ICE		
	nd mathemat																
-	ectives: Stud				-			_	_		_	_					
	fects. It cove		_	-					-			tiai amp	onners	, and	oper	ation	a
amplifiers. Emphasis is placed on performance metrics, gain enhancement, and stability techniques. Course Outcome: After completion of the course, the student will be able to													Bloom's Knowledge Level (KL)				
CO1	Analyze MOSFET small signal models including channel length modulation and back gate effects. K 2																
CO2	Design cur	rent soui	ces, mir	rors, an	d voltag	ge/curre	nt refer	ences.						K5			
CO3	Implement													K4			
CO4	Analyze tw					•			ation.					К3			
CO5	Compare a		•			ete-tim	e compa	arators.						K1			
CO-PO Mag CO-PO Mapping	pping (Scale PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSC	D2 PSO3		3	
CO1	3	3	-	2	2	-	-	-	-	1	-	3					
CO2	3	2	3	-	2	-	-	-	-	-	-	3					
CO3	3	3	3	2	2	-	-	-	-	-	-	3					
CO4	3	3	3	3	2	-	-	-	-	1	-	3					
CO5	3	3	-	2	2	-	-	-	-	1	2	3					
	tents / Syllal	ous															
Module 1			Bas	sic MO	S Devi	ice Phy	ysics									8 hour	'S
	Гransistor, F									nnel len	gth mo	dulatio	n and	back	gate	effec	:t
evaluation (Module 2	of figure of	merit fo			der dif Mirror										1	8	_
									_							hour	
	ch, MOS Di generation,																
Module 3 Differential Amplifiers												8 hour	S				
	oifferential A	•	ers, Case	code A	mplifie	ers, Cu	rrent A	mplifie	ers, Ou	ıtput Ar	nplifier	s, High			1		
Module 4 OP-AMP												8 hour	••				
	tics of ideal	•	ional an	nplifie	c, const	ituents	of op	-amp,	small	signal a	nalysis	of 2 st	age o	p-an			_
Module 5	ana somunon	io.	Con	mpara	tor											8 hour	·s
Characteriz	ation of Co	mparato	or. Two	-Stage	. Open	-Loop	Comp	arators	, Othe	r Open	-Loop	Compai	rators.	. Im			

		Total Lecture Hours	40						
Textbook			hours						
S.No	Book Title with publication agency & year	Author							
1	Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition	Behzad Razavi,							
2	Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013	David A. Johns, Ken Martin,	Wiley						
Reference	Books:	<u>.</u>							
S.No	Book Title with publication agency & year	Author							
1	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010	Philip E. Allen and Douglas R. O. Holberg							
2	Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.	Geiger, Allen and Stradder							
NPTEL/	Youtube/ Faculty Video Link:								
1	https://www.youtube.com/watch?v=qf49IvJNsGM								
2	https://www.youtube.com/watch?v=PHmrsLfPS8Y								
3	https://www.youtube.com/watch?v=JvS-VNDGHV0								
4	https://www.youtube.com/watch?v=HIe7Ne6kMo8	https://www.youtube.com/watch?v=HIe7Ne6kMo8							
	https://www.youtube.com/watch?v=Anj8OYXAY20								

Course Code: BEC0402N	Course Name: Microprocessor & Microcontroller	L	T	P	C
Course Offered in: VLSI		3	0	0	3

Pre-requisite: : Basics of digital electronics

Course Objectives: Students will learn about:

- **1.**The fundamentals of general microprocessor & microcontroller.
- 2. The fundamentals of 8086 microprocessor.
- 3. The architecture of 8051 microcontroller with real time application.
- 4. The fundamentals of ARM Processor and embedded systems.
- 5. The knowledge of ARM Instruction Set for programming.

Course	Course Outcome: After completion of the course, the student will be able to					
		Level (KL)				
CO1	Explain the fundamentals of general microprocessor & micro-controller	K 2				
CO2	Explain the fundamentals of 8086 microprocessor.	K5				
CO3	Implement 8051 microcontroller for designing various applications.	K4				
CO4	Illustrate the fundamentals of ARM Cortex M0 Processor.	К3				
CO5	Apply the knowledge of ARM Instruction Set for programming.	K1				

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	1	2	3	2
CO2	3	3	2	-	-	-	-	-	-	-	1	3	3	2
CO3	3	3	3	-	-	-	-	-	-	-	1	2	3	2
CO4	3	3	3	-	-	-	-	-	-	-	1	2	3	2
CO5	3	3	3	-	-	-	-	-	-	-	1	2	2	2

Course Contents / Syllabus

Module 1 Fundamentals of Microprocessors and Computer Architecture

8 hours

History and Evolution of Microprocessor and microcontrollers, Computer architecture: Harvard & Von Neumann architecture, RISC & CISC architecture, Different Layers of computer architecture, Buses, types of buses, bus architecture, Microprocessor architecture and its operations, address and data bus Multiplexing and Demultiplexing, Instruction format and size.

Module 2 8086 Microprocessor Architecture and Programming

8 hours

Introduction to 8086 – Microprocessor architecture, Pipelining Concept, Memory Segmentation, General Purpose Registers, Pointer And Index Registers, Flag Register, Bus Interface Unit, 8086 Pin Description, Addressing modes ,Instruction set and assembler directives , 8086 Interrupt -Software and Hardware Interrupts

Module 3

8051 Microcontroller: Architecture, Programming, and Applications

8 hours

Overview of the 8051, Inside the 8051, Addressing modes, 8051 data types and directives, Instruction set and assembly language programming of 8051 microcontrollers, Programming the 8051 timers, Interfacing of I/O devices (keypad & display) with 8051. Application of 8051 microcontroller

Module 4

ARM Cortex-M Series: Architecture and Cortex-M0 Fundamentals

8 hours

Arm Processor Families, Arm Cortex-M Series Family, Cortex-M0 Processor: Cortex-M0 Overview, Cortex-M0 Block Diagram, Cortex-M0 Three-stage Pipeline, Cortex-M0 Registers, Cortex-M0 LR, Cortex-M0 PSRs, Cortex-M0 Memory Map, Cortex-M0 Executable Memory Space, Cortex-M0 Device Memory Space, Cortex-M0 Private Peripheral Bus, Cortex-M0 Reserved Memory Space, Cortex-M0 Memory Map Example, Cortex-M0 Endianness.

Module 5

Cortex-M0 Instruction Set and Low-Power Features

8 hours

Thumb Instruction Set, Thumb-2 Instruction Set, Cortex-M0 Instruction Set, Register Access: The Move Instruction, Memory Access: The LOAD Instruction, The STORE Instruction, Stack Access: PUSH and POP, Arithmetic instructions (ADD, SUB, MUL, CMP),

Logic Operation, Arithmetic Shift Operation, Logical Shift Operation, Rotate Operation, Reverse Ordering Operation, Sleep Mode Related Instructions, CortexM0 Low Power Features: Sleep Mode, Sleep-on-Exit Feature, How to Enable Sleep Features, Processor Wakeup Conditions, Wakeup Interrupt Controller, Enter and Exit Deep Sleep Mode

		Total Lecture Hours 40 hours					
Textboo	k:						
S.No	Book Title with publication agency & year	Author					
1	Ramesh Gaonkar, "Microprocessor Architecture, Programming, and	Ramesh Gaonkar					
	Applications with the 8085", 5th Edition, Penram International Publication						
	(India) Pvt. Ltd.						
2	Douglas V. Hall, "Microprocessors and Interfacing", Tata McGraw Hill	Douglas V. Hall,					
Ref	erence Books:						
S.No	Book Title with publication agency & year	Author					
1	Mazidi Ali Muhammad, Mazidi Gillispie Janice, and McKinlay Rolin D	Mazidi Ali Muhammad					
•	"The 8051	Maziai / III Mailaililiaa					
2	Microcontroller and Embedded Systems using Assembly and C", Pearson	Pearson					
	Publication.						
3	ARM system developers guide, Andrew N Sloss, Dominic Symes and Chris	Andrew N Sloss					
	Wright, Elsevier, Morgan Kaufman publishers, 2008.						
NPTEI	/ Youtube/ Faculty Video Link:						
1	https://www.youtube.com/watch?v=xBYhHC8_A60	_					
2	https://www.youtube.com/watch?v=cNN_tTXABUA						
3	https://www.youtube.com/watch?v=sLW1TptEJBQ						
4	https://www.youtube.com/watch?v=9zOo4JkZgSI						
5	https://www.youtube.com/watch?v=Anj8OYXAY20						
5	nttps://www.youtube.com/watch?v=Anj8OYXAY20						

Course	Code:	BECVL04	112		Cor	urse Na	ame: Da	ita Ana	lytics					L	T	P	C
Course	Offere	d in: VLS	I											3	0	0	3
Pre-req	uisite:	: Basics of	f digital o	electroni	cs.												
Course	Object	tives: Stud	ent will	learn abo	out Vari	ious bas	sic conc	epts & 1	undam	entals	of Data a	analytics	s. They v	vill lear	n va	rious	types
		and their	-		•	ll unde	rstand E	Explorat	ory dat	a analy	sis and	visualiz	ation tec	hniques	s and	d will	learr
		eau progra															
Course	Outco	me: After	completi	on of the	e course	, the stu	udent w	ill be ab	le to					Blooi Level		Know! L)	ledge
CO1		erstand the		ental con	icepts o	f data a	nalytics	in the a	reas th	at play	s major 1	ole with	nin the	K 2			
CO2	Expl	ain and ex	emplify t	he most	commo	n form	s of data	and its	represe	entatio	ns.			K5			
CO3	Appl	y data pre-	-processi	ng techn	iques o	n hetero	ogenous	dataset	s.					K4			
CO4	Anal	yze data u	sing expl	oratory	data ana	alysis								К3			
CO5	Apply visualization tool to analyze and draw inference from different types of data sets w.r.t different application scenarios. Mapping (Scale 1: Low, 2: Medium, 3: High)																
CO-PO	Mapp	ing (Scale	1: Low,	2: Med	ium, 3:	High)	T	1	1	ı	1	1	1	1			
CO-PO		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	2	PSO3	•
CO1		3	2	-	-	-	-	-	-	-	2	-	-	-		2	
CO2	CO2		2	-	2	3	-	-	-	-	-	-	2	3		-	
CO3		-	3	2	3	3	-	-	-	-		-	3	3		-	
CO4		-	3	3	-	3	-	-	2	2	2	-	-	3		2	
CO5		-	-	3	-	3	-	-	2	2	-	-	2	2		-	
		nts / Sylla									_						
Module			oundatio													8 hou	
		Data Scier ools and to															
		cations of															Dan
Module		D															rs
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		SV file, im iance, SD,	•			•											
Module			ata Pre													8 hou	
			ransforn	-	_				•			Ç,		O,			
Form of	Data P	re-process	ing, data	Attribut	e and its	s types,	underst	anding	and ext	racting	useful v	ariables	, KDD, p	rocess,	Data	a Clea	ning
		s, Noisy D															
		n and Tran															
Adjusted R-Square, Significance of p-value, Introduction to data visualization and various graphical ways of da Module 4 Advanced Data Cleaning, Transformation, and Exploration									ata repr		8 hou						
					ndant variables, variable Selection, identifying outliers, Removing									Outlie			
	-	transforma		_						•	_		_				
-		ar Discrii			-			_		_	_		-				-
		Is and oth		-						_	-		J			<i>U U</i> ,	
Module			ata Visu							<u> </u>						8 hou	rs
Getting	g starte	and overvi	oleau So	ftware, U	Using D												
	I ree m	naps), Usir	ig the Sh	ow me r	anel.												

Tableau Calculations: Overview of SUM, AVR, and Aggregate Features Creating custom calculations and fields, Applying new data calculations to your visualization. Manipulating Data in Tableau: Cleaning-up the data with the Data Interpreter, structuring your data, Sorting, and filtering Tableau data, Pivoting Tableau data. Advanced Visualization Tools: Using Filters, Using the Detail panel Using the Size panels, customizing filters, Using and Customizing tooltips, formatting your data with colors, Creating Dashboards & Stories, Distributing & Publishing Your Visualization

		Total Lecture Hours 40 hours							
Textbool	Κ:	·							
S.No	Book Title with publication agency & year	Author							
1	Text Books:, Making sense of Data: A practical Guide to Exploratory Data	Glenn J. Myatt							
	Analysis and Data Mining, John Wiley Publishers, 2007								
2	Data Analysis and Data Mining, 2nd Edition, John Wiley & Sons	John Wiley & Sons							
	Publication, 2014.								
3	Open Data for Sustainable Community: Glocalized Sustainable	Neha Sharma, Santanu Ghosh							
	Development Goals, Neha Sharma, Santanu Ghosh, Monodeep Saha,								
	Springer, 2021								
Refe	rence Books:								
S.No	Book Title with publication agency & year	Author							
1	The Data Science Handbook, Field Cady, John Wiley & Sons, Inc, 2017	John Wiley & Sons							
2	Data Mining Concepts and Techniques, Third Edition, Jiawei Han,	Jiawei Han							
	Micheline Kamber, Jian Pei, Morgan Kaufmann, 2012.								
NPTEL	Youtube/ Faculty Video Link:								
1	https://www.youtube.com/watch?v=xBYhHC8 A60								
2	https://www.youtube.com/watch?v=cNN_tTXABUA								
3	https://www.youtube.com/watch?v=sLW1TptEJBQ								
4	https://www.youtube.com/watch?v=9zOo4JkZgSI								
5	https://www.youtube.com/watch?v=Anj8OYXAY20								

Course	Code:	BECVL0	413		Cor	urse Na	me: Io	T Arch	itectui	re and	Protoc	ols		L	ГР	С
Course	Offere	d in: VLS	I		•									3 () 0	3
Pre-req	uisite:	: Basic kn	owledge	of IoT											•	
Course	Object	ives: Stud	ent will	learn abo	out:											
1.	The ar	chitectural	l overvie	w and Io	T refer	ence are	chitectu	re								
2.	The op	en-source	architec	cture and	design	princip	les.									
3.		rious type				otocols.										
		ent types o	-	_												
		ences betw												1 .		
Course	Outcor	ne: After	completi	on of the	e course	, the stu	ident wi	ll be ab	le to					Bloom'		ledg
	I													Level (KL)	
CO1	Expla	in the arcl	hitectura	l overvie	ew and I	lo'I' refe	rence m	iodel.						K 2		
CO2	Demo	onstrate the	e IoT ref	ference a	rchitect	ure.								K5		
CO3	Analy	yze the var	rious typ	es of IoT	connec	ctivity p	rotocol	S.						K4		
CO4	Expla	in the diff	erent typ	pes of Io	T layere	ed proto	cols.							К3		
CO5	Desci	ribe the dif	fferences	s between	n Web o	of thing	s and In	ternet o	f Thing	gs.				K1		
СО-РО	 Mappi	ing (Scale	1: Low,	2: Med	ium, 3:	High)										
CO-PO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3	2
Mappi	ng	101	102	103	104	103	100	107	100	10)	1010	1011	1301	1302	150.	,
CO1		3	2	1	2	2	1	2	1	-	2	1	2	3	2	
CO2		3	2	3	2	3	2	2	2	1	2	2	3	3	2	
CO3		3	2	2	3	3	2	1	1	-	1	1	2	3	2	
CO4		3	2	3	3	3	2	2	2	1	2	2	2	3	2	
CO5		2	1	1	1	2	3	2	2	1	1	1	2	2	2	
		nts / Syllal	ous												,	
Module															8 hou	
		ctural Ove														
		inctional V ints- Intro														
		r Network		Technic	ai Desig	sii const	1411165, 1	Jaia Ic _f	resente	uion an	ia visaai	ızatıon,	meracu	on and re	mote co	nuo
Module															8 hou	rs
		e architec														
		k - Overvi cific to NE		ivity sta	ck archi	tecture-	- Kesou	rce mod	iel and	Abstra	ction. L	oRawA	N archit	ecture, Cl	nannel a	cces
Module		CITIC TO INI	5-101												8 hou	rs
		ty Overvie	ew. Wire	eless Lor	ng Rang	e (WA	N) Prote	ocols, I	AN Pr	otocols	s. Serial	Protoco	ls. IoT t	ransmissi		
		otocols, Fe						<u> </u>			<u></u>		,			
Module	4														8 hou	rs
Protocol	Standa	ardization	for IoT,	Efforts,	M2M a	nd WS	N Proto	cols, SO	CADA	and RF	ID Prote	ocols, Is	sues wit	h IoT Sta	ndardiz	atio
Unified '		andards Pr			2.15.4, I	EEE 80	2.11, B	AC Net	Protoc	ol Mod	lbus, KN	X, arch	itecture a	and Protoc	col stack	use
		work layer	, APS la	yer												
in Zig be	5														8 hou	
in Zig be Module		versus Int									ardizatic	n for W	oT, Plat	form Mic	ldleware	of to
in Zig be Module Web of			JOT Area	hitaatiira		THE PARTY A	nu Dusi	11022 111	migell	CC						
in Zig be Module Web of		Multitier W	VoT Arc	hitecture	, WOIF	Ortais a			<u> </u>			Tota	l Lectui	re Hours	40 ho	urs
in Zig be Module Web of	nified N		VoT Arc	hitecture	, worr	ortuis u						Tota	ıl Lectui	re Hours	40 ho	urs

1	Honbo Zhou, "The Internet of Things in the Cloud: A Middleware	Honbo Zhou
•	Perspective", CRC Press, 2012	Hono Zhou
2	Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds),	Dieter Uckelmann
_	"Architecting the Internet of Things", Springer, 2011	Dieter Gekennann
3	David Easley and Jon Kleinberg, "Networks, Crowds, and Markets:	David Easley and Jon Kleinberg
	Reasoning About a Highly Connected World", Cambridge University Press,	Buvia Easiey and von Fremeerg
	2010.	
Referenc	e Books:	
S.No	Book Title with publication agency & year	Author
1	Vijay Madisetti and ArshdeepBahga, "Internet of Things (A Hands-on-	Vijay Madisetti
	Approach)",1st Edition, VPT, 2014.	
2	Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach	Francis daCosta
	to Connecting Everything", 1st Edition, Apress Publications,2013	
NPTEL	Youtube/ Faculty Video Link:	
1	https://www.youtube.com/watch?v=xBYhHC8 A6o	
-		
2	https://www.youtube.com/watch?v=cNN_tTXABUA	
3	https://www.youtube.com/watch?v=sLW1TptEJBQ	
4	https://www.youtube.com/watch?v=9zOo4JkZgSI	
T	https://www.youtube.com/watch:v=/20043kZgSi	
	https://www.youtube.com/watch?v=Anj8OYXAY20	

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		BECVL0			Co	urse Na	me: Co	mpour	nd Sem	icondu	ictors				Г Р	C	
		d in: VLS												3	0 0	3	
		: Basic kr															
	•	t ives: Thi											_				
		application		_									will del	ve into the	ne fabri	cation	
_		ce physics								d semi	conducto	ors.		Т			
Course	Outcor	ne: After	completi	on of the	e course	, the stu	ident w	ill be ab	le to						's Know	ledge	
														Level (KL)		
CO1	Com	prehensivo	e Unders	tanding o	of Com	oound S	Semicon	ductor l	Materia	ls				W 2			
														K 2			
CO2	Devi	ce Physics	s of Com	pound So	emicono	ductor								K5			
	Fobri	cation Te	chniques	and Pro	200000:									I K3			
CO3	1 4011	cation 10	cimiques	and 1100	cesses.									K4			
CO4	Appl	ications in	n Electron	nic and C	Optoelec	ctronic I	Devices										
CO4														K3			
CO5	Emer	ging Tech	nnologies	and Tre	nds in (Compou	ind Sem	icondu	ctors					K1			
	Mapping (Scale 1: Low, 2: Medium, 3: High)													K1			
CO-PO	Mapp	ing (Scale	: 1; Low,	, 2: Mea	lum, 3:	nigii)					I			1			
СО-РО		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO:	3	
Mappir	ng									2 0 2		1 011		1502			
CO1		3	1	2	2		-	-	-	-	-	-	2	2	1		
CO2		3	1	2	1	1		-		_	_		2	2	1		
l -			+	1		1										_	
CO3		3	1	2	2	1	-	-		-	-	-	2	2	1		
CO4		3	1	3	2	1	-	-	-	-	-	-	2	2	1		
CO5		3	1	2	2	1	-	-	-	-	-	-	2	2	1		
Course	Conter	nts / Sylla	bus	•	•	•	•	•	•		•				•		
Module	1														8 hou	ırs	
Overviev	w of c	ompound	semico	nductors	and th	neir sig	nificanc	e, Hist	orical	context	t and ev	olution	of com	pound s	emicono	luctor	
		troduction	1 to key c	ompoun	d semic	onducto	or mater	rials							1		
Module															8 hou		
		es and pro									ental sem	icondu	ctors. De	vice phys	sics prin	ciples	
		pound ser	niconduc	tors. Hig	gh-speed	d transis	stors and	d integra	ated cir	cuits							
Module															8 hou		
Principle diodes (I		application	ons of op	otoelectro	onic de	vices us	sing coi	npound	semic	onduct	ors. Lase	ers, pho	todetect	ors, and	lıght-en	ntting	
Module															8 hou	ırc	
		h techniq	ues for co	ompound	Lsemico	nducto	re Lithe	aranhy	and et	ching r	rocesses	specifi	c to com	nound se			
Module		ii teening	101 00	Jiipoune	Schille	maucto	15. Little	Jerupiry	and co	cimig p	70003303	specifi	e to com	pound se.	8 hou		
		f compou	nd samia	ondusto	ra in hi	ah frag	uonou d	ovi oos	Miorox	vovo t	rongistors	and o	mmuni	nation day			
		and trends							MICION	wave u	ansistors	s and co	Jiiiiiiuiii	ation de	vices. L	aiesi	
de velopi	iiciitis t	ina trentas	ти сотпр	ouria ser	meonau	ictor tee	mioros.	<i>)</i>				Tota	ıl Lectui	e Hours	40 ho	ours	
Textboo	k:														I		
S.No		ok Title w	vith publ	ication a	agency	& year					Aut	hor					
1	_	YungChe				-					Keh	YungC	heng				
		ompound	_	ductorsa	ndDevi	ces.Spri	nger,20	20.				-	-				
2		o W.Pohl.							cation o	of	Udo	W.Poh	ı1.				
		erostructu				•											
3			*														
Refe	erence	Books:									ı.						

S.No	Book Title with publication agency & year	Author
1	. Gupta, S.Optoelectronicdevicesandsystems.PHILearningPvt.Ltd.,2014	Gupta, S
2	Birtalan, Dave. Optoelectronics. CRC Press, 2018	Birtalan, Dave.
NPTEL/	Youtube/ Faculty Video Link:	
1	https://www.youtube.com/watch?v=xBYhHC8 A6o	
2	https://www.youtube.com/watch?v=cNN_tTXABUA	
3	https://www.youtube.com/watch?v=sLW1TptEJBQ	
4	https://www.youtube.com/watch?v=9zOo4JkZgSI	
5	https://www.youtube.com/watch?v=Anj8OYXAY20	

Course	Cod	e: BAS()403			Course	Name: A	Advance	ed Engin	eering N	Tathema	itics		L	T	P	С
Course	Offe	red in:	B.Tech.		•									3	1	0	4
Pre-req	uisit	e: B.Te	ch 1st ye	ar													
Course	Obje	ectives:	The obje	ctive of	this cours	se is to fa	miliariz	e the stu	dents wit	h concep	ts of stat	istical te	chnique	s, co	mple	x var	iables
	-								l concept	-			-		-		
of mathe	emati	ics and a	application	ons that v	would be	essentia	l for the	ir discip	lines.								
Course	Outo	come: A	fter com	pletion	of the cou	urse, the	student	will be a	ble to					Bloo	m's k	now	ledge
				•											l (KL		Č
CO1	Ap	ply the	concept	of skewr	ess and	Kurtosis	in the re	elevant a	pplication	n area.					K	.3	
CO2	Ap	ply the	concept	of Rando	m Varia	ble and l	Probabili	ity Distr	ibutions i	in real w	orld prob	olems.			K	.3	
CO3									analytic						K		
CO4	-		concepts integrals		lex func	tions for	finding	Taylor's	series, L	aurent's	series ar	nd evalua	ation		K	3	
CO5					r Transf	orm to s	olve eng	ineering	problem	S.					K	3	
CO-PO	Map	pping (S	Scale 1: l	Low, 2:]	Medium	, 3: Higl	h)										
CO-PO		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	P	SO2	PSO3	
CO1	<u>-</u> 8	3	2	2	3	1	1	_	1	2	2	2	2		1		-
CO2		3	2	2	3	1	1	-	1	2	2	2	2		1		-
CO3		3	2	1	2	-	-	-	-	1	1	1	2		1		-
CO4		3	2	2	3	-	-	-	-	2	1	1	2		1		-
CO5		3	2	2	3	1	-	-	-	2	1	1	2		1		-
Course		tents / S	Syllabus														
Module	1			Sta	tistical T	Cechniqu	ies-I								8	3 hou	rs
Introduc	tion:	Measu	res of c	entral te	ndency:	Mean,	Median,	Mode,	Standard	deviati	on, Quar	tile dev	iation,	Mon	nent,	Skew	ness,
Kurtosis																	
Module	2			Rar	ndom Va	riables	and dist	tribution	1						1	l0 ho	urs
									Variable omial, Po			ndom Va	ariable,	Expe	ected	Valu	e of a
Module		,	,		nplex Va					, ,					1	0 ho	urs
		nuity and	d differe						Analytic	functions	s. Cauch	v- Riema	nn eau	ation			
			ic functi									,	•		`		
Module	4			Cor	nplex Va	ariable -	-Integra	tion							1	l0 ho	urs
_		_		_	-				ement), C	-	_				-		
					•		_	s, Classi	fication of	of Singu	larities, z	eros of a	nalytic	func	tions.	Resi	dues,
		inding r	esidues,														
Module	5			Inte	egral Tra	ansform	S								1	l0 ho	urs
Complex	x Fou	ırier traı	nsform, I	Inverse T	ransforn	ns, Conv	olution '	Theorem	s, Fourie	r sine an	d cosine	transfor	m.				
												Total L	ecture	Hou	rs	18 ho	urs
Textboo											_						
S.No		Book Ti									Autho						
1		Textbook of Engineering Mathematics- IV									Bali, N						
2		Advanced engineering mathematics										R.K.					
3		Higher engineering mathematics										ıl, B.S.					
4	S	Statistica	ıl methoc	ds							Gupta	, S.P.					
5	A	Advance	d engine	ering ma	thematic	es					ZILL,	DENNI	S G.				
Referen	ce B	ooks:															
S.No	TP	Book Tit	tle								Autho	r					
D-1140		JUN III									Auult	71					

1	Introduction to Probability Models	Ross, Sheldon M
2	Probability, Random Variables and Stochastic Processes	Papoulis, Athanasios
3	Advanced engineering mathematics	Kreyszig, E.
NPTEL/	Youtube/ Faculty Video Link:	
Module 1	https://youtu.be/1MiT06JFNo4?si=zVH-5AdAeu7Qcs9x https://youtu.be/6lQn1hdG43o?si=2WJXQHXJE-ByAghk https://archive.nptel.ac.in/courses/110/107/110107114/	
Module 2	https://archive.nptel.ac.in/courses/111/104/111104032/	
Module 3	https://archive.nptel.ac.in/courses/111/107/111107056/	
Module 4	https://archive.nptel.ac.in/courses/111/103/111103070/	
Module 5	NPTEL :: Mathematics - NOC:Integral Transforms And Their Ap	pplications

LAB Course Code: BEC0452	LAB Course Name: Microprocessor & Microcontroller Lab	L	T	P	С
Course Offered in: VLSI		0	0	4	2

Pre-requisite: Basics of digital circuits.

Course Objectives: Students will learn about

- 1. The fundamentals of general microprocessor & microcontroller.
- 2. The fundamentals of 8086 microprocessor.
- 3. The architecture of 8051 microcontroller with real time application.
- 4. The fundamentals of ARM Processor and embedded systems.
- 5. The knowledge of ARM Instruction Set for programming.

Course	Outcome: After completion of the course, the student will be able to	Bloom's Knowledge
		Level (KL)
CO1	Apply the knowledge of Microprocessor for writing assembly level language	К3
CO2	Implement timer in 8051 microcontroller for generating waveforms	К3
CO3	Analyze the interfacing of various I/O devices with programming	K4
CO4	Apply the knowledge of ARM Instruction Set to write the program for given application	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-I O Map	Jang (Start	1								1				
CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	3	2	3	-	-	-	-	2	-	3	3	1
CO2	3	3	3	2	3	-	-	-	-	1	-	3	3	1
CO3	3	3	3	2	3	-	-	-	-	1	-	3	3	1
CO4	3	3	3	3	3	-	-	-	-	2	1	3	3	2

List Of Practical's (Indicative & Not Limited To)

To study 8086 microprocessor system

Write a program using 8086 Microprocessor for Hexadecimal addition of two 8-bit Numbers

Write a program using 8086 Microprocessor for Hexadecimal subtraction of two 8-bit Numbers

Write a program using 8086 Microprocessor for Hexadecimal addition of two 16-bit Numbers

Write a program using 8086 Microprocessor for Hexadecimal subtraction of two 16-bit Numbers

Write a program using 8086 Microprocessor for addition of two BCD numbers

Write a program using 8086 Microprocessor for subtraction of two BCD numbers

To perform multiplication of two 8-bit numbers using 8086.

To perform division of two 8-bit numbers using 8086

To find the smallest number in an array of data using 8086 instructions set

To find the largest number in an array of data using 8086 instructions set

To write a program to arrange an array of data in ascending order using 8086

To write a program to arrange an array of data in descending order using 8086

To convert given ASCII number in to its equivalent Hexadecimal number using 8086 instructions set

To convert given Hexadecimal number in to its equivalent ASCII number using 8086 instructions set

Write a program to find smallest and largest number in the array using 8051 microcontroller

Write a program to arrange numbers in ascending and descending order using 8051 microcontroller

Write a program to find addition and subtraction of two 8 bit numbers using 8051 microcontroller.

Write a program to find multiplication and division of two 8 bit numbers using 8051 microcontroller

Write a program to square of a 8 bit numbers using 8051 microcontroller.

Write a program to cube of a 8 bit numbers using 8051 microcontroller

Write a program of flashing LED connected to port of the 8051 microcontroller

Write a program to generate 10 kHz square wave using 8051 microcontroller

Write a program to generate a Ramp waveform of 1 KHz using DAC with 8051 micro controller

Write a program to show the use of INT0 and INT1 of 8051 microcontrollers

Interfacing of sensors and display devices like Serial Communication Code, Bluetooth, seven segments with 8051 microcontrollers

Inte Write and simulate a program for data transfer using ARM freedom board.rfacing of Relay & Stepper Motor with 8051 microcontrollers.

Write and simulate a program for arithmetic operations using ARM freedom board.

Write and simulate a program for logical operations using ARM freedom board

Write a program for Interfacing of temperature sensor with ARM freedom board (or any otherARM microprocessor board) and display object temperature on LCD

Write an embedded C program to blink the LED with time delay intervals using LPC2148 ARM microcontroller

Write an embedded C program to read switch status and display in LED using LPC2148 ARM microcontroller.

Write an embedded C program to ON/OFF buzzer with time delay intervals using LPC2148 ARM microcontroller

Write an embedded C program generate a square wave using internal 10 bit DAC using LPC2148 ARM microcontroller

Write an embedded C program generate a triangular wave using internal 10 bit DAC using LPC2148 ARM microcontroller.

Write an embedded C program generate a PWM waveform using LPC2148 ARM microcontroller

Write an embedded C program to transmit and receive data from PC using UART serial port using LPC2148 ARM microcontroller.

Write an embedded C program to read on-chip ADC value of temperature sensor LM35 and display in hyper terminal using UART1 using LPC2148 ARM microcontroller

Write an embedded C program to read the external interrupts INT1 and INT2 and display in hyper-terminal using UART1 using LPC2148 ARM microcontroller

Write an embedded C program to toggle relays with delay intervals using LPC2148 ARM microcontroller

Write an embedded C program to control the stepper motor using LPC2148 ARM microcontroller

LAB Course Code: BECVL0452	LAB Course Name: CMOS Analog Integrated Circuit Lab	L	T	P	С
Course Offered in: VLSI		0	0	2	1

Pre-requisite: Basic understanding of electronic devices, circuit theory, and operational amplifiers. Familiarity with SPICE simulation and mathematical tools like differential equations is also recommended.

Course Objectives: Student will learn about analog CMOS circuit design, focusing on small signal modeling of MOSFETs and their non-ideal effects. It covers the design and analysis of current mirrors, CMOS amplifiers, differential amplifiers, and operational amplifiers. Emphasis is placed on performance metrics, gain enhancement, and stability techniques.

Course	Course Outcome: After completion of the course, the student will be able to					
		Level (KL)				
CO1	Analyze the electrical characteristics of MOSFETs and extract design parameters	К3				
CO2	Design and simulate CMOS amplifier stages (CS, CG, Cascode) using EDA tools	К3				
CO3	Implement and evaluate differential amplifiers and current mirrors	K4				
CO4	Analyze the frequency response of amplifier circuits and interpret results	K4				
CO5	Design, simulate, and layout advanced op-amp architectures like telescopic and folded cascode.	K5				

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

СО-ГО Марр	ning (Beare	1. LUW,	Z. Micui	um, J.	ingii)					1				1
CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	-	2	2	-	-	-	-	1	-	3	2	-
CO2	3	2	3	-	2	-	-	-	-	-	-	3	2	-
CO3	3	3	3	2	2	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	2	-	-	-	-	1	-	3	3	-
CO5	3	3	-	2	2					1	2	3	3	2

List Of Practical's (Indicative & Not Limited To)

Study of MOS Characteristics and Characterization

Design a CMOS Inverting Amplifier.

Design and Simulation of Single Stage Common Source Amplifiers

Design and Simulation of Single Stage Common Gate Amplifiers

Design and Simulation of Single Stage Cascode Amplifier Amplifiers

Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)

Design and Simulation of Basic Current Mirror

Design and Simulation of Cascode Current Mirror

Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier

Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

LAB Co	ourse :	Code BE	C0455		LAB Course Name: Verilog-HDL (Departmental Workshop II)								L	T	P	(
Course	Offere	d in: VLS	Ī											0	0	6	3
Pre-req	uisite:	Hardware	coding la	anguage													
		tives: The			luce the	partici	pants to	the ver	ilog ha	rdware	descript	ion lang	guage. It	will he	lp th	nem to	
	-	igital circui				-	•		-		-	_			•		
		me: After of		_										Bloo	m's i	Knowl	ed
			•											Leve			•
CO1	Deve	lop and ide	entify the	e suitable	e abstrac	ction le	vel for a	narticu	ılar dig	ital des	ign				- '	<u></u>	_
CO2		lop verilog														K3	
CO3		lop verilog												K4			
CO4		gn and veri									es			K4			
CO5	Desig	gn and sim	ulate bas	ic modu	les usin	g switcl	h level 1	nodelin	g.					K5			
C O-PO	Марр	ing (Scale	1: Low,	2: Medi	ium, 3:	High)											
CO-PO Mappii		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO	2	PSO3	
CO1		3	2	2	-	3	-	-	-	-	2	1	3		-		2
CO2		3	3	2	-	3	-	-	-	-	2	1	3		-		-
CO3		3	2	2	-	3	-	-	-	-	2	1	3		2		-
																	_

3

CO4

CO5

	Course Contents/Syllabus					
	Evolution of CAD, emergence of HDLs, typical HDL-flow, trends in HDLs, Verilog vs VHDL, Verilog coding vs Software Programming.					
Unit-1	Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.					
	Lexical conventions, data types: value set, registers, vectors, arrays, strings, system tasks, compiler directives.	15 Hour				
	Module definition, port declaration, connecting ports, hierarchical name referencing					
Unit-2	Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.	15 Hour				
UIIIt-2	Continuous assignments, delay specification, expressions, operators, operands, operator types.	13 HOUI				
Unit-3	Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.	20 Hour				
Unit-4	Timing and Delays, Switch-Level Modeling, Logic Synthesis with Verilog HDL, Specify block and Timing checks, Verification and Writing test benches, Timing Analysis of Logic circuits, Downloading of verilog code in FPGA and CPLD.	20 Hour				

Unit-5	Concept of switch level abstraction, MOS Transistor as Switch, Modeling NMOS and PMOS transistors as switches in Verilog, Switch ON/OFF conditions and control signals, Verilog Switch-Level Primitives, Understanding Verilog switch primitives: nmos, pmos, Syntax and usage of switch primitives in Verilog code.	20 Hour

List of Practical

Lab	Program Logic Building	СО
No.		Mapping
1	Simulate and synthesize following logic gates using gate level modeling a) AND Gate b) OR Gate c) NOT Gate d) EX-OR Gate e) NAND Gate f) NOR Gate	CO1
2	Simulate and synthesize following combinational circuits using gate level modeling a) Half adder b) Full adder c) Half subtractor d) Full subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 Demultiplexer h) 2:4 Decoder i) 1 Bit Comparator j) 2*2 Bit Multiplier	CO2
3	a) Simulate and synthesize binary to gray code converter using gate level modeling.b) Simulate and synthesize gray to binary code converter using gate level modeling.	CO 2
4	Simulate and synthesize following combinational circuits using data flow modeling a) Half adder b) Full adder c) Half subtractor d) Full subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 Demultiplexer h) 2:4 Decoder i) 1 Bit Comparator j) 2*2 Bit Multiplier	CO 2
5	Simulate and synthesize 4 bit parallel adder/subtractor using data flow modeling.	CO 2
6	Simulate and synthesize following ALU operations using data flow modeling	CO 2

	OPCODE	ALU Operation							
	1.	A+B	_						
	2.	A-B							
	3.	A Complement							
	4.	A*B							
		gray code converter using dainary code converter using da							
Simulate a	and synthesize following flip	flops using behavioral mode	ling						
			COS						
a) Using	and synthesize flip flops using positive edge and negative synchronous and asynchronous	edge.	COS						
		ft registers using behavioral r	nodeling						
a) Serialb) Serialc) Parall	input serial output input parallel output el input serial output el input parallel output		COS						
	* *	versal shift register using bel	navioral modeling CO3						
2 Simulate a	and synthesize following cou	inters using behavioral mode	ing						
a) 2 Bit ofb) Mod sc) Decaded) Ring of	Counter 5 Counter de Counter Counter on Counter		COS						
		ier using behavioral modeling	; CO3						
4	and synthesize 4:1 MUX by	using 2:1 MUX	CO3						
b) Using	; a reg								
a) 1									
Simulate a a) 1	orr and synthesize Mealy sequer 010 011	nce	CO3						
7 Implemen	tation of logic gates on an F	PGA and verify gates function	nality.						
8 Implemen	tation of 4:1 multiplexer on	a FPGΔ	CO						

19	mplementation of 2*2 multiplier on a FPGA							
20	Implementation of D flip flop on a FPGA	CO 4						
21	Design and simulation of CMOS inverter using switch level modeling CO 5							
22	Simulate and synthesize following logic gates using switch level modeling a) AND Gate b) OR Gate c) NOT Gate d) EX-OR Gate e) NAND Gate f) NOR Gate	CO 5						

Required Software and Tools (Any one) ISE Simulator (Xilinx) / Xilinx Vivado

- Verilog-XL (Cadence)
- VCS ('big 3') (Synopsys)

LAB Course Code: BCSCC0452	LAB Course Name: Problem Solving Approaches	L	T	P	С
Course Offered in: IV SEM		0	0	2	1

Pre-requisite: Programming Language C/C++ or Java or Python

Course Objectives:

Problem-solving in computer programming involves a structured approach to identifying, analyzing, and resolving coding challenges. The process typically includes thoroughly understanding the problem, decomposing it into smaller, manageable parts, designing an appropriate algorithm, implementing the solution through code, and performing testing and debugging to ensure correctness and efficiency

CITICICITY						
Course	Course Outcome: After completion of the course, the student will be able to					
		Level (KL)				
CO1	Develop logic-based solutions using control statements and recursion to solve basic and intermediate computational problems.	K6				
CO2	Apply bit manipulation techniques to find efficient solutions for binary and low-level operations.	K3				
CO3	Implement and manipulate arrays and strings using fundamental and advanced searching sorting techniques.	K3				
CO4	Utilize algorithmic strategies to optimize solutions for complex problem scenarios.	K3				
CO5	Analyze and debug code for logical errors and improve the efficiency of the solution using appropriate data structures and algorithmic patterns.	K4				

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5		PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	-	-	-	2	-	-	-	-	-	-
CO2	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO3	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO4	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO5	3	3	2	2	-	-	-	2	-	-	-	-	-	-

List Of Practical's (Indicative & Not Limited To)

Problem Statements need to be discussed in lab session: Control Statements

1. Secure Password Generator

A company wants to create a secure password generator for their employees. The password must be based on specific numeric properties to enhance its complexity and security. Write a program to validate and generate a secure password according to the following rules:

1. Prime Number Validation:

- The user must input a 3-digit number. The program should first check if the number is a prime number.
- If it is not a prime number, the user should be prompted to enter another number until a valid prime number is provided.

2. Sum of Digits Check:

• Once a valid prime number is entered, calculate the sum of its digits. If the sum of the digits is not divisible by 3, ask the user to enter another prime number until a valid one is found.

3. Armstrong Number Check:

• Check entered prime number is Armstrong or not? If Armstrong are found, prompt the user to enter another prime number and repeat the process.

Password Generation:

Concatenate the 1 if entered prime number is Armstrong otherwise 2 with the sum of the digits of the valid prime number to form the secure password.

Example Scenario:

Sample Input

Enter a 3-digit prime number: 153

Sum of digits of 153 = 9The sum is divisible by 3. 153 is Armstrong number

Sample Output

Secure Password: 19

2. Write a function to input electricity unit charges and calculate total electricity bill according to the given condition:

For first 50 units Rs. 0.50/unit

For next 100 units Rs. 0.75/unit

For next 100 units Rs. 1.20/unit

For unit above 250 Rs. 1.50/unit

An additional surcharge of 20% is added to the bill

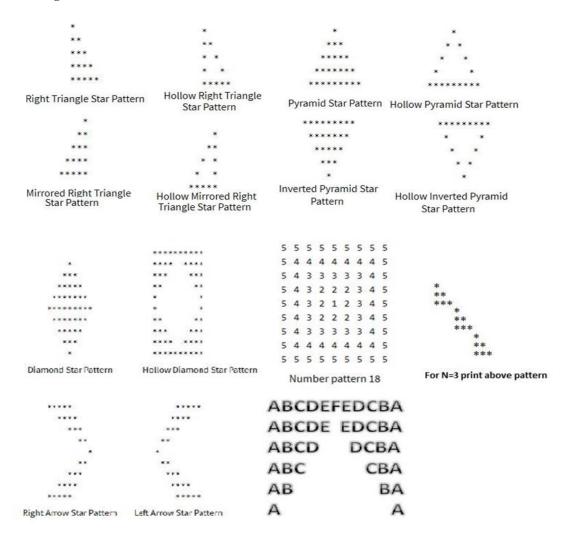
3. Write a method to generate a secure code which the sum of all possible palindrome numbers between given two numbers.

For Example: **Input**: 10, 80 **Output**: 308

Explanation: All palindrome numbers between 10 & 80 are: 11,22,33,44,55,66,77

Password= 11+22+33+44+55+66+77 = 308

4. Draw the following Patterns for N=5



Problem Statements need to be discussed in lab session: Recursive Approach (Basic)

1. Write a program that takes an integer n as input and prints the multiplication table of n from n * 1 to n * 10. The output should clearly show each multiplication step.

2. Write a program to calculate the sum of all integers from 1 to a given number N. The program should take N as input and output the total sum using iteration or recursion.

3. Find the GCD of Two Numbers Using Recursion:

Write a recursive function to calculate the Greatest Common Divisor (GCD) of two numbers using Euclid's algorithm. The function should take two integers as input and return their GCD.

4. Find the LCM of Two Numbers Using Recursion:

Write a program to compute the Least Common Multiple (LCM) of two numbers using recursion. You may use the relationship LCM(a, b) = |a * b| / GCD(a, b) and a recursive function for GCD.

Problem Statements need to be discussed in lab session: Bit Manipulation

- 1. Write a program to count the number of set bits (1s) in the binary representation of a given integer. The program should efficiently use bitwise operations to perform the task without converting the number to a string.
- 2. Write a program that takes a number and a bit position as input and checks whether the bit at that position is set (1) or clear (0). Use bitwise operators to perform the check
- **3.** Given a number and a position, write a program to toggle (invert) the bit at the given position using bitwise operations. The result should reflect the updated value of the number after flipping the bit.
- **4.** Write a program to compute the XOR of all numbers from 1 to n using a mathematical pattern (not a loop). Use bitwise XOR properties to achieve an efficient solution.
- 5. Given an array of size n-1 containing unique elements from 1 to n, find the missing number using bit manipulation (preferably XOR approach) without sorting or using extra space.
- **6.** Given an array where all elements repeat twice except two elements that appear only once, write a program to find the two non-repeating elements using bitwise operations in linear time and constant space.
- 7. Write a program to check if a given number is a power of two using bit manipulation. A number is a power of two if it has exactly one set bit in its binary representation.
- **8.** Given two integers A and B, write a program to count how many bits need to be flipped to convert A to B. Use XOR to find differing bits and count the number of set bits.
- **9.** Write an efficient program to count the total number of set bits in binary representations of all numbers from 1 to n. Optimize the approach using bitwise logic and recursion.
- **10.** Write a program to calculate the square of a number using only bitwise operations and addition. Do not use multiplication, division, or any power functions.
- 11. Write a function to add two integers using bitwise operations only. Avoid using the + or operators. Implement logic using XOR and AND operations for binary addition.
- **12.** Write a program to generate the power set (all subsets) of a given set using bitwise representation. Each subset can be represented by a binary number where each bit indicates inclusion of the corresponding element.

Problem Statements need to be discussed in lab session: Arrays (Try to use sliding window, prefix sum, cadence, recursion, bit manipulation, two pointer approaches)

- 1. Sarah is assisting the "MathMinds Club" in creating passwords for their online platform. They have a list of numbers, some stable and some unstable. Define a function that can help Sarah calculate the password according to the given scenario. Scenario:
 - There are N numbers provided.
 - A number is stable if each digit appears the same number of times.
 - A number is unstable if the frequency of its digits is not the same.
 - The password is computed as the sum of all stable numbers minus the sum of all unstable numbers.
 - Consider only those numbers in the list that have more than equal to three digits.

For example:

Input: N=5 List: 12, 1313, 122, 678, 898

Output: Password: 971

2. Given an array of integers, including possible negative values, you are allowed to modify at most one element by doubling its value. The goal is to find the maximum possible sum of any subarray after making this modification.

Input:

arr = [-2, 1, -3, 4, -1, 2, 1, -5, 4]

Expected Output:

- Original Maximum Subarray Sum: 6 (achieved from [4, -1, 2, 1])
- Maximum Sum After Modification: 10(achieved from [8, -1, 2, 1], where the value 4 is doubled to 8).
- **3.** For a given string, generate a pattern based on the following rules:

Input: A string of characters (e.g., "HAT").

Output: Generate patterns by replacing characters with the numeric value 1 and process the patterns as described below:

- 1. Replace one character at a time with 1:
 - o For each character in the string, replace it with 1, keeping the other characters unchanged.
 - Example for "HAT": 1AT, H1T, HA1
- 2. Replace two characters at a time with 1:
 - Replace every combination of two characters with 1, keeping the remaining character unchanged.
 - o If 1s are consecutive, replace them with their sum (e.g., 11T becomes 2T).
 - Example for "HAT":

 $11T \rightarrow 2T$, $H11 \rightarrow H2$, 1A1

- 3. Replace all characters with 1:
 - o Replace all characters in the string with 1.
 - o If there are consecutive 1s, sum them up (e.g., 111 becomes 3).
 - o Example for "HAT":

 $111 \rightarrow 3$

Final Output

For the string "HAT", the output should be:

1AT, H1T, HA1, 2T, H2, 1A1, 3.

4. Given a sorted array arr [] and a target value, the task is to count triplets (i, j, k) of valid indices, such that arr[i] + arr[j] + arr[k] = target and i < j < k.

Examples:

Input: arr[] = [-3, -1, -1, 0, 1, 2], target = -2

Output: 4

- **5.** You are given an array prices[] where prices[i] represents the price of a given stock on day i. You want to maximize your profit by choosing a single day to buy one stock and choosing a different day in the future to sell that stock. Write a program to return the maximum profit you can achieve from this transaction. If no profit is possible, return 0.
- 6. Find the "Kth" max and min element of an array:

Given k, find the k-th smallest and k-th largest element in the array.

Input: arr = [7, 10, 4, 3, 20, 15], k = 3 Output: Kth Smallest: 7, Kth Largest: 10

7. Sort a binary array with values 0, 1, and 2 using constant space and one pass (Dutch National Flag algorithm).

Input: [0, 2, 1, 2, 0]Output: [0, 0, 1, 2, 2]

8. Find **longest consecutive subsequence:**

Return the length of the longest consecutive elements sequence.

Input: [1, 9, 3, 10, 4, 20, 2] Output: 4 (Sequence: 1, 2, 3, 4)

9. Given a number of bits and a number K. In one flip you can toggle exactly K consecutive bits. With only this flip operation available, convert the string into all 1.

Input String: 0000110000 and K=3

Following are four flip operations by using which all bits converted into 1's.

Flip1-1110110000 Flip2-1110110111 Flip3-1111000111 Flip4-111111111

If it is not possible to convert all bits into one's then print "IMPOSSIBLE".

10. Given a list of non-negative integers, arrange them in such a way that they form the largest possible number. Since the result can be very large, return it as a string in **O(N log N)** time complexity.

Example-1	Example-2
Input:	Input:
N = 5	N = 4
Arr[] = {3, 30, 34, 5, 9}	Arr[] = {54, 546, 548, 60}
Output: 9534330	Output: 6054854654

11. Given an array arr[] of size n containing distinct integers within the range [1, n+2], find the two missing numbers from the first n+2 natural numbers.

Constraints:

- The solution must run in O(N) time and use O(1) extra space.
- The array does not contain duplicate values.

Examples:

Input: arr[] = [1, 2, 4, 6, 3, 8], n = 6

Output: 5, 7

12. Given a string str of lowercase alphabets and a number k, the task is to print the minimum value of the string after removal of k characters. The value of a string is defined as the sum of squares of the count of each distinct character present in the string. Return the minimum possible required value. **Examples:**

Input: str = "abccc", k = 1

Output: 6

Input: str = "aabcbcbcabcc", k = 3

Output: 27

Expected Time Complexity: O(n+klog(p))

Note: Here n is the length of string and p is number of distinct alphabets and k number of alphabets to be removed.

13. Given a non-negative integer **S** represented as a string, remove **K** digits from the number so that the new number is the smallest possible.

Note: The given *num* does not contain any leading zero.

Expected Time Complexity: O(|S|).

Example 1:	Example 2:	
Input:	Input:	
S = "149811", K = 3	S = "1002991", K = 3	
Output:	Output:	
111	21	

14. You are given a two-dimensional grid board[][] of size n * m consisting of English letters and a string target. Your task is to determine whether the target word can be formed by sequentially connecting letters from the grid. You may move to adjacent cells horizontally or vertically (not diagonally), and a cell may not be reused once it is part of the current path.

Examples:

Input:

 $board[][] = [['C', \, 'A', \, 'T'], \, ['R', \, 'A', \, 'K'], \, ['T', \, 'O', \, 'N']],$

target = "CART"

Output: true

Explanation:

You can trace the word "CART" through the path: $C \to A \to R \to T$ (moving horizontally and vertically, without repeating cells).

- **15.** Given an encoded string **s**, the task is to decode it. The encoding rule is:
 - **k[encodedString]**, where the **encodedString** inside the square brackets is being repeated exactly **k** times. Note that **k** is guaranteed to be a positive integer, and encodedString contains only lowercase english alphabets.

Note: The test cases are generated so that the length of the output string will never exceed 10⁵.

Examples:

Input: s = "1[b]" **Output:** "b"

Input: s = "3[b2[ca]]" **Output:** "bcacabcacabcaca"

*Competitive coding list will be shared with the students.

Total Hours: 30 hrs.

Course	se Code: BNC0402 Course Name: Environmental Science L T							P	C					
Course	Offere	d in: All the branches 2 0							0	2	_			
Pre-req	uisite:]	Basic kno	wledge of	biology, cl	hemistry, e	cology, ge	ology, mat	hematics, a	and underst	tanding	of h	uman	impacts on	
natural s	ystems	•												
Course	Outcor	ne- After	completio	n of the co	urse, the st	udent will	be able to						Bloom's	
understa	nd ecos	systems, p	promote su	stainability	, address e	nvironmer	ntal issues,	conserve b	oiodiversity	, and		Kı	nowledge Level	
ensure re	esponsi	ble use of	natural re	sources for	future gen	erations.							(KL)	
CO1	Understand the basic principles of ecology and environment. Ecosystem: Basic concepts, K1,K2													
CO1	comp	components of ecosystem, food chains and food webs. Ecological pyramids, biodiversity.												
CO2	Understand the different types of natural recourses like food, forest, Minerals and energy and their								K1,K2					
CO2	conse	rvation.	ion.											
CO3	Understand the different types of pollution, pollutants, their sources, effects and their control								K1,K2					
	metho	methods.												
CO4	Understand the basic concepts of sustainable development, Environmental Impact Assessment									K1,K2				
	(EIA) and different acts related to environment													Ц
CO-		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO	9	PO	10 PO11	
Mappi		2	2	2	2		2	2	2	2				4
CO1	l	3	3	2	2		3	3	2	2			2	
CO2	<u>, </u>	3	3	2	2		3	3	2	2			2	_
				_	_				_	_				
CO3	3	3	3	2	2		3	3	2	2			2	
COA	1	3	3	2	2		3	3	3	2	-		2	_

Course Contents / Syllabus

Module 1 Basic Principle of Ecology and Biodiversity

5 hours

Definition, Scope and basic principles of ecology and environment. Ecosystem: Basic concepts, components of ecosystem. Food chains and food. Webs. Ecological pyramids, Energy flow in ecological systems, Characteristics of different ecosystems. Biogeochemical Cycles: Importance, gaseous and sedimentary cycles. Carbon, Nitrogen, Phosphorus and Sulphur Cycles. Biodiversity and their importance, Threats to biodiversity, major causes, extinction's, vulnerability of species to extinction, IUCN threat categories, Red data book. Strategies for biodiversity conservation, principles of biodiversity conservation in-situ and ex-situ conservation strategies Mega diversity zones and Hot spots, concepts, distribution and importance.

Module 2 Natural Resources and Ecological succession

5 hours

Natural resources and associated problems. Forest resources: Use and over- exploitation, deforestation. Timber extraction, mining, dams and their effects on forest and tribal people. Mineral resources: Use and exploitation, environmental effects of extracting and using mineral resources. Food resources: World food problems, changes caused by agriculture and over- grazing, effects of modern agriculture, fertilizer-pesticide problems, water logging, and salinity. Land resources: Land as a resource, land degradation, man induced landslides. Equitable use of resources for sustainable lifestyles.

Non-Renewable Energy Resources: Fossil fuels and their reserves, Nuclear energy, types, uses and effects, Renewable Energy Resources: hydropower, Solar energy, geothermal, tidal and wind energy, Biomass energy, biogas and its advantages. Ecological succession-Types, stages, examples of ecological succession

Module 3 Pollution and Waste Management

5 hours

Air pollution: sources of air pollution, Primary and secondary air pollutants. Origin and effects of SOX, NOX, Cox,CFC, Hydrocarbon, control of air pollution. Water pollution: sources and types of water pollution, Effects of water pollution, Eutrophication, Soil pollution: Causes of soil pollution, Effects of soil pollution, Major sources of and effects of noise pollution on health, Radioactive and thermal pollution sources and their effects on surrounding environment. Solid waste disposal and its effects on surrounding environment, Introduction to E- Waste, Types and classification of E- Waste, Impacts of E- Waste on environment and human health, E-Waste management and recycling., Climate change, global warming, acid rain, ozone layer depletion.

Module 4

Environmental Assessment and Legislation

5 hours

Women education, Role of NGOs regarding environmental protection, Bio indicators and their role, Natural disasters and disasters

management, Aims and objectives of Environmental Impact Assessment (EIA). Salient features of following Acts: Environmental Protection Act, 1986, Wildlife (Protection) Act, 1972. Water (Prevention and control of pollution) Act, 1974. Forest (Conserving) Act, 1980.

Definition and concept of sustainability, impacted areas of sustainable development, Global initiative and issues on sustainable development UNSDsGs, System Thinking and Sustainability.

	Total Lecture Hours 20 h						
Textbook:							
S.No	Book Title	Author					
1	Brady, N.C. 1990. The nature and properties of Soils, Tenth Edition. Mac Millan Publishing Co., New York	Brady, N.C					
2	Sodhi G.S. 2005, Fundamentals of Environmental Chemistry: Narosa Publishing House, New Delhi.	Sodhi G.S					
3	Dash, M.C. (1994), Fundamentals of Ecology, Tata Mc Graw Hill, New Delhi.	Dash, M.C					
		•					
S.No							
1	Rao M.N. and H.V.N. Rao, 1989 : Air Pollution, Tata McGraw Hill Publishing Co. Ltd., New Delhi	Rao M.N. and H.V.N. Rao					
2	A Text Book of environmental Science By Shashi Chawla	Shashi Chawla					
Unit 1:	https://www.youtube.com/watch?v=T21OO0sBBfc, https://www.youtub	oe.com/watch?v=qt8AMjKKPDo					
Unit 2:	https://www.youtube.com/watch?v=mOwyPENHhbc, https://www.youtube.com/watch?v=yqev1G2iy2 https://www.youtube.com/watch?v= 74S3z3IO I, https://www.youtube.com/watch?v=jXVw6M6m2						
Unit 3:							
Unit 4	https://www.youtube.com/watch?v=ad9KhgGw5iA, https://www.youtube.com/watch?v=nW5g83NSH9 M, https://www.youtube.com/watch?v=xqSZL4Ka8xo						
	https://www.youtube.com/wutch:v-Aqbziz-fixuoAb						